Crosstalk Noise Modeling for Coupled SWCNT Bundle Interconnects using MRTD Technique

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Abstract: This paper analyzes the crosstalk effects of resistive driven single-walled carbon nanotube (SWCNT) bundle interconnects. The wavelet-based numerical model Multiresolution Time Domain (MRTD) approach is used for interconnects analysis. The performance of the proposed model MRTD against the traditional Finite Difference Time Domain (FDTD) model and the SPICE tool is used to evaluate the global interconnects at 32nm technology node. Mathematical equations are done using MATLAB. For various test cases, the effect of line resistances on crosstalk effects were evaluated for delay measurement, while in-phase, out-phase and functional crosstalk, the average errors is observed to be less than 2.9%, 1.86% and 1.78% respectively, and also the estimated noise peak voltage, is less than 1 percent on average. In that observation, proposed MRTD model dominates the traditional FDTD as accurately as the results of the SPICE simulation. This approach can be used to resolve the problems of electromagnetic interference and electromagnetic compatibility of on-chip interconnects.

Keywords: SWCNT bundle interconnects, Delay, Peak crosstalk noise, FDTD, MRTD

1. Introduction:

In nanoscale technology nodes, the latest Copper on-chip interconnects fails to comply with the specifications. The speed and reliability of high-density copper wires on-chip is reduced due to the Joule heating, surface, and grain boundary scatterings [1]. The features of carbon nanotubes (CNTs) have made them promising materials with applications to VLSI circuits, and both CNTs and graphene's nanotubes are being explored as alternate materials for interconnect solutions [2].

CNTs can be multi-walled carbon nanotubes (MWCNTs), double-walled, and single-walled. CNTs are formed by rolling graphene sheets into a hollow cylindrical

shape. CNTs may act as semiconductors, or they may have metallic properties depending on how they are rolled. SWCNT with a single graphene layer can be rolled up with a diameter as of 0.4nm to 4nm. MWCNT and DWCNT are two and several concentric graphene sheet shells that are wrapped together. Crosstalk results have been studied for DWCNT and SWCNT interconnects in [3]. The isolated SWCNT has a parasitic high impedance in [4] and a distinction is made between the Cu and the monolayer SWCNT interconnects. It has been observed that isolated SWCNT are sluggish. A bundle of SWCNT is used to solve this restriction. And the general impedance of the SWCNT interconnect bundle decreases. The number of current conduction and conduction channels [5] is also increased. It is studied in [4],[6] that the output of the bundle SWCNTs can be more crucial than the copper interconnects in terms of less delay in the propagation of the circuit. It is also been shown that accuracy of the SWCNT bundle can improve as the interconnects length increases or technology scaled down [7].

Previous models [8], [9] viewed the non-linear CMOS driver as a simply linear resistor in order to analyse crosstalk noise, which seems to deviate from the effects. For the transient period, the MOSFET functions at about half of its capacity in the saturation; afterwards, it operates at linear (or) cutoff regions. For the DIL system, a number of techniques using various analytical solutions, the Finite Difference Time Domain (FDTD) approach, and SPICE findings have been reported in recent publications in [10]-[12].

The FDTD method was applied for CNT interconnects in [13]–[16]. When comparing MWCNT interconnects to Cu interconnects for crosstalk noise research, Liang et al. [13] employed the FDTD technique, and it was found that the nonlinear CMOS driver is a linear resistive driver. However, the model's HSPICE validation was not discussed. In addition to analysing HSPICE as a linear resistive driver with the nonlinear CMOS driver, Kumar et al. [14] investigated the inclusion crosstalk noise of FDTD, two-coupled MWCNT interconnects. FDTD approach to a nonlinear CMOS driver using the modified alpha-power law model in order to investigate crosstalk noise in coupled MWCNT interconnects [15],[16].

The numerical distributive approach known as FDTD [17] is employed for propagation along the discretisation. Therefore, a model with an advantage in numerical distribution qualities is desperately needed. A multi-resolution time domain (MRTD) method with the added benefit of the numerical dispersion characteristics has been proposed by Krumpholz and Katehi [17], [18], and [19]. Grivet-Talocia [20] proposed the MRTD model, which provides the same precision as the FDTD model, using the Haar Scaling function as a fundamental function. Additionally, Fujii et al. [21] presented the MRTD technique, which is more accurate than the FDTD system, as a fundamental function based on Daubechies' scaling function and involves

three and four extinguished moments. Tong et al. [22] introduced an MRTD model for transient analysis of two-conductor transmission lines with excellent numerical dispersion. Characteristics and enhanced accuracy with SPICE in comparison to the FDTD model. In addition, Rebelli and Nistala in [23]–[25] proposed using the MRTD approach to assess the signal integrity of a coupled Copper interconnect controlled by a nonlinear CMOS and a linear resistive that is reliant on the Daubechies scaling function at four extinct moments.

A numerical model is suggested in this paper and is based on the MRTD model for functional crosstalk and dynamic crosstalk analysis of coupled transmission lines driven by linear resistance. The most effectives time domain's analysis is presented for coupled transmission lines based on SWCNT bundle interconnects. Due to the delay caused by line resistances on crosstalk induced, peak voltages are analyzed under dynamic crosstalk as well as propagation delay and noise peak voltages for functional crosstalk. The obtained results using a MRTD model is compared with the FDTD and SPICE tool as well.

The rest of the paper is organised as follows. The electrical modelling of the SWCNT bundle's interconnects is covered in Section 2. Section 3 discusses the transmission line-based MRTD model, and Section 4 presents the MRTD Model Comparisons and Evaluation. Finally, section 5. conclusions are given.

2. Bundled SWCNT Interconnects Modeling:

The hexagonal graphene's sheets rolled up into hollow cylinders are SWCNTs. They consists of a single shell with diameter ranges from 0.33nm to 5nm and length from 2nm to 10nm.This section provides a detailed descriptions of the modeling of the SWCNT bundled interconnects

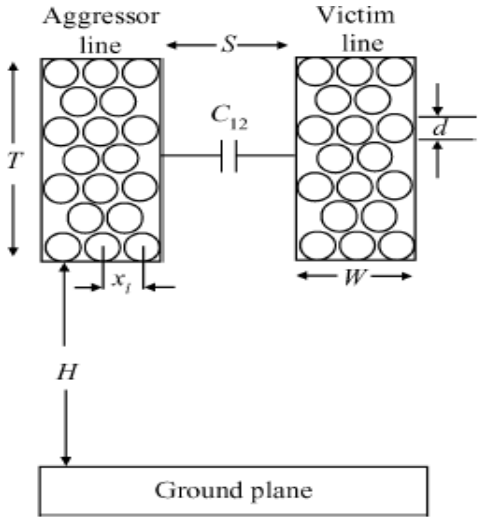


Figure 1. Structure of coupling SWCNTs bundle interconnects.

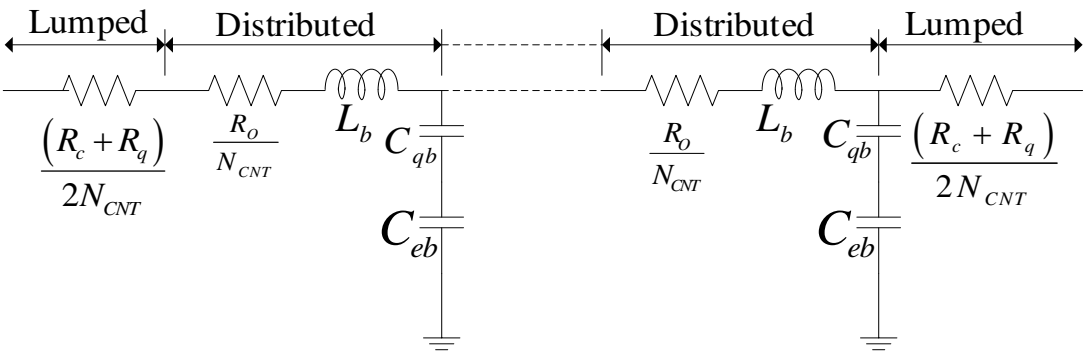


Figure 2. The ESC model of SWCNT bundle interconnect structure

2.1 Structure, parasitic components and equivalent model of capacitive coupling bundle SWCNT interconnect

The parallel combination of hexagonally bundled equal metallic SWCNTs forms a bundle. Each SWCNT has six immediate neighbors and is uniformly divided by the 'xi' inter-CNT distance. The structure of the interconnects SWCNT bundle is illustrated in Figure 1. In this case, The T/W aspect ratio is equivalent to 3. The d diameter of SWCNT for a high-density bundle is considered to be equal to the inter-CNT distance. W is width and T is thickness and S is the separations of the adjacents SWCNT bundles which interconnects the lines. H is the heights of the bundle of the ground plane. Suppose the thickness is equal to the height and the separation equal to the width for the bundle structure. N_T and N_W are the number of SWCNTs bundle along the thickness and width of the SWCNTs bundle respectively.

It is possible to express total number of SWCNTs bundle as [26]

$$N_{CNT} = N_W N_T - \frac{N_T}{2}, \qquad N_T \text{ is even} \qquad (1a)$$

$$N_{CNT} = N_W N_T - \frac{(N_T-1)}{2}, \qquad N_T \text{ is odd} \qquad (1b)$$

where $N_W = \text{int}\left[\frac{W-d}{x_i}\right]$; $N_T = \text{int}\left[\frac{T-d}{\frac{\sqrt{3}}{2}x_i}\right]+1$

The electrical circuits model for the bundled SWCNT distributed R,L,C interconnect is illustrated in Figure 2. SWCNT bundled modeling interconnects with the parasitic inductance, resistance, and capacitance mentioned in this subsection [27]

2.2.1 Bundle SWCNT interconnect of Resistance

Bundle SWCNT interconnect resistance Rb can be defined [27] as

$$R_b = \frac{R_{CNT}}{N_{CNT}} \qquad (2a)$$

Where R_{CNT} is isolated SWCNT's overall resistance, and it can be expressed as

$$R_{CNT} = R_c + R_q\,,\ l < \lambda \qquad (2b)$$

$$R_{CNT} = R_c + R_q + R_o\,,\ l \gg \lambda \qquad (2c)$$

where, l is length of the SWCNT bundle, λ is free path for electron, R_c is metal nanotubes contact resistance,

$$R_c = \frac{h}{4e^2}$$

R_q is quantum resistances, and Ro is dependent ohmic resistance. The effect of the metal-nanotube Rc contact resistances is omitted in this proposed analysis.

$$R_o = \frac{R_q l}{\lambda}$$

2.2.2 Bundle SWCNT interconnect of Inductance

To obtain the inductance L_b in [27] as

$$L_b = l\frac{L_{CNT}}{L_{CNT}} \qquad (3)$$

Where L_{CNT} is inductance in *p.u.l* of an isolated SWCNT.

2.2.3 Bundle SWCNT interconnect of Capacitance

The Cb capacitance of the SWCNT bundle interconnects of the l length is a combination in series of its C_{eb} electrostatic capacitance, and C_{qb} quantum capacitance. It can be represented [27] as

$$C_b = l\frac{C_{qb}C_{eb}}{C_{qb}+C_{eb}} \qquad (4a)$$

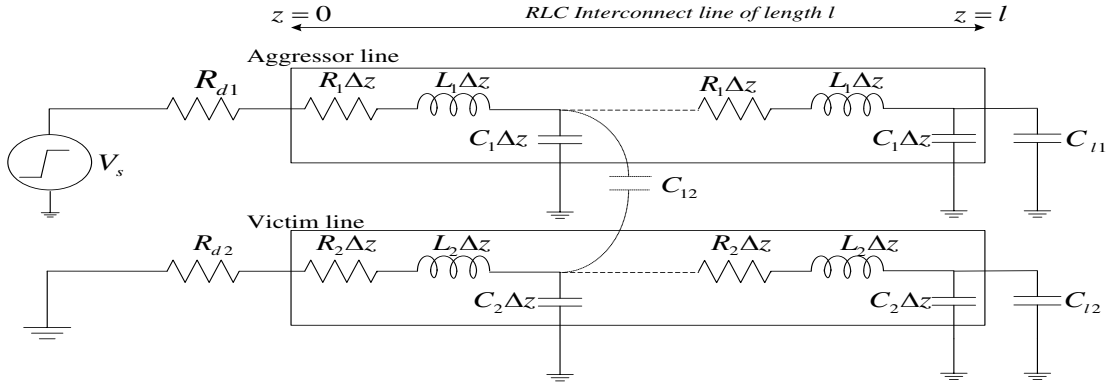
where C_{eb} and C_{qb} are electrostatic capacitance and quantum capacitance of *p.u.l*

If S and d are the separation and diameter of SWCNT bundle respectively, If S>>d, then the Cc coupling capacitance *p.u.l* is between two Bundle SWCNTs interconnects can be defined [28]as

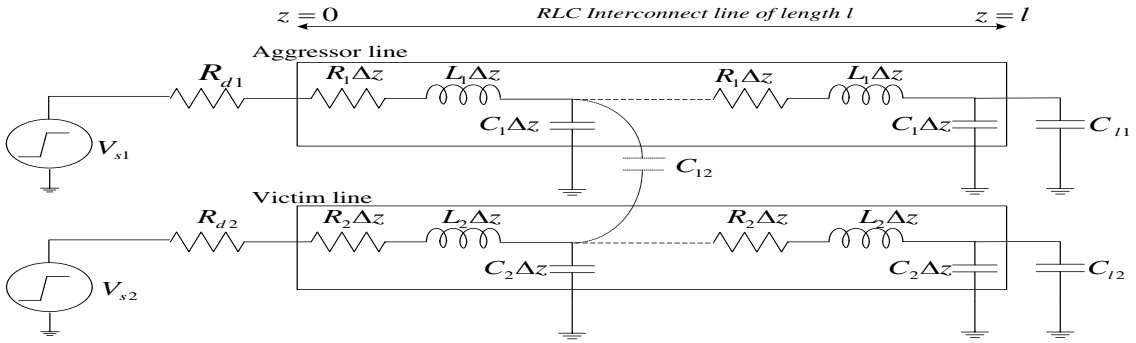
$$C_c = \frac{\pi\varepsilon}{\ln(2S/d)} \qquad (4b)$$

3. MRTD Model based on transmission lines:

The capacitively coupled transmission lines which are built on the SWCNT bundle interconnects are illustrated in Figures 3(a), 3(b), and 3(c). C_{12} is coupling capacitance *p.u.l* between two interconnects lines. C_1, R_1, L_1, and C_2, R_2, L_2 are capacitances, resistances, inductances *p.u.l* through aggressor line and victim line, respectively. The mutual conductance and inductance between two interconnects line are very insignificant and it can be neglected in the paper. The capacitance load across the victim's and aggressor's lines is represented by C_{l1} and C_{l2}, respectively. Every line of length l is driven by an equivalent resistives through a voltages source at z=0 and terminated by a capacitance load at z=l.

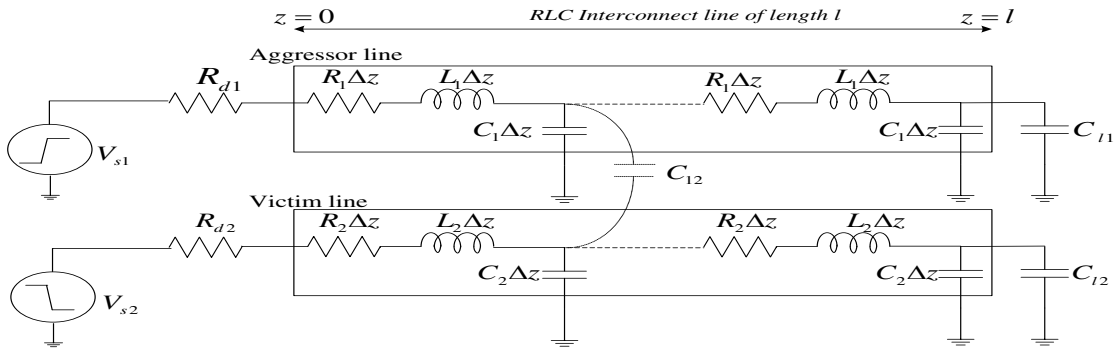


3(a)



3(b)

3(



c

)

Figure 3. Capacitive coupled 2- interconnects line for 3(a) functional 3(b) in-phase and (c) out-phase switching.

Telegrapher's TEM-mode equations [29] can be used to model the coupled on-chip interconnects.

$$\frac{\partial V(z,t)}{\partial z} = -RI(z,t) - L\frac{\partial I(z,t)}{\partial t} \qquad (5a)$$

$$\frac{\partial I(z,t)}{\partial z} = -C\frac{\partial V(z,t)}{\partial t} \qquad (5b)$$

'Z' and 't' signify place and time, respectively. In 2×1 matrices, the currents and voltages values are obtained in 2×2 square matrices, and the parasitic R, L, and C are provided. The separate formulae for parasitic R, L, C, V, and I matrices are

$$V = \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}_{2\times1} I = \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}_{2\times1}; R = \begin{bmatrix} R_1 & 0 \\ 0 & R_2 \end{bmatrix}_{2\times2}; L = \begin{bmatrix} L_1 & 0 \\ 0 & L_2 \end{bmatrix}_{2\times2}; C = \begin{bmatrix} C_1 + C_{12} & -C_{12} \\ -C_{12} & C_2 + C_{12} \end{bmatrix}_{2\times2}$$

In this case, line 1 is related to by subscript 1, and line 2 by subscript 2. The measurement sites for voltage and current on bundle SWCNT interconnects line 1 are shown in Figure 4.

As an alternative, telegrapher equations are evaluated by taking into account current and voltage points in both space and time. As seen in Figure 4, where Δt is time and Δz is space depicted in discretisations intervals, the currents and voltages are separated by Δt/2 in time and Δz/2 in space for improved precision.

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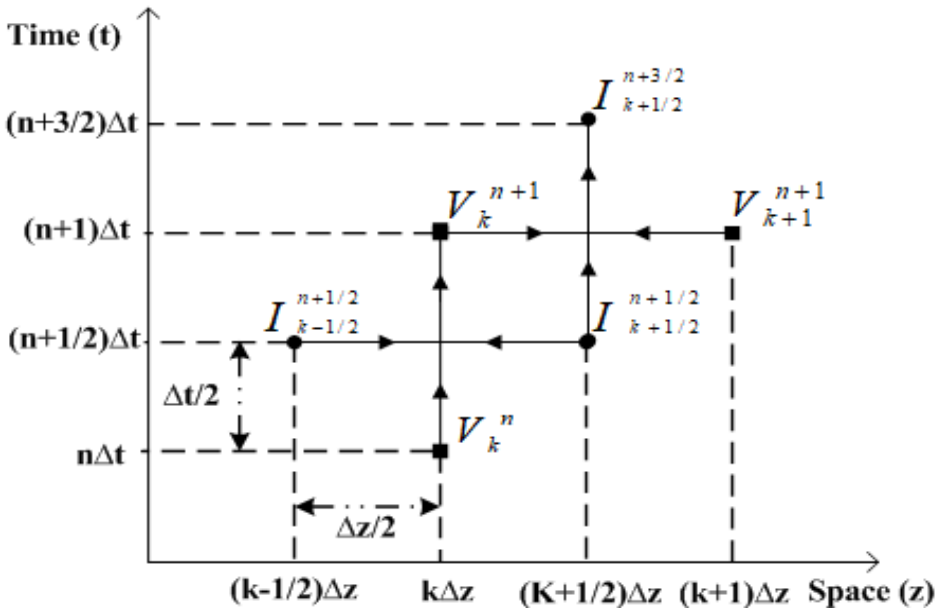

Figure4. Space and time discretizations on bundle SWCNT interconnect line.

A capacitive load is terminated at z = l, and the connecting line l of length is a resistive driver at z = 0. Figure 5 shows that the line is constantly separated into NDZ segments of length Δz=l/NDZ, revealing the discretisation voltage (V) and current (I) nodes, which are coefficients of unknown. Source current is represented by Io in this figure.

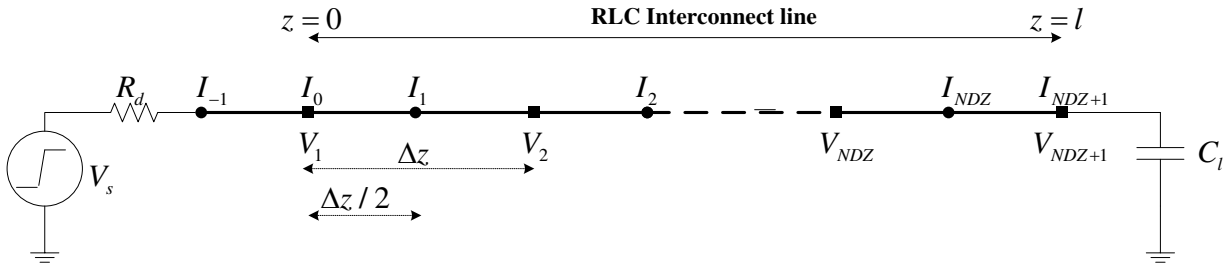

Figure5. I and V's spatial discretisation on the bundle SWCNTs interconnect line.

The known functions (hn(t) and Φk(z)) can be used to extend the terms for voltages and currents. the coefficients of unknown in order to use the procedure outlined in [19] to solve equations (5a) and (5b):

$$V(z,t) = \sum_{k,n=-\infty}^{+\infty} V_k^n \emptyset_k(z) h_n(t) \quad (6a)$$

$$I(z,t) = \sum_{k,n=-\infty}^{+\infty} I_{k+\frac{1}{2}}^{n+\frac{1}{2}} \emptyset_{k+\frac{1}{2}}(z) h_{n+\frac{1}{2}}(t) \quad (6b)$$

The definitions of function hn(t) and $\Phi_k(z)$ are:

$$h_n(t) = h\left(\frac{t}{\Delta t} - n\right) \quad (7a)$$

The definition of the pulse function h(t) is

$$h(t) = \begin{cases} 1 & \text{for } |t| < \frac{1}{2} \\ \frac{1}{2} & \text{for } |t| = \frac{1}{2} \\ 0 & \text{for } |t| > \frac{1}{2} \end{cases} \quad (7b)$$

$$\emptyset_k(z) = \emptyset\left(\frac{z}{\Delta z} - k\right) \quad (7c)$$

The scaling function of a Daubechies is denoted by Φ(z), and the Haar scaling function is represented by h(t).

The MRTD approach for equations (5a) and (5b) is derived by taking into account the following integrals [30]:

$$\int_{-\infty}^{+\infty} h_n(t) h_{n'}(t)\, dt = \delta_{n,n'} \Delta t \quad (8a)$$

$$\int_{-\infty}^{+\infty} h_n(t) \frac{\partial h_{n'+\frac{1}{2}}}{\partial t} dt = \delta_{n,n'} - \delta_{n,n'+1} \quad (8b)$$

$$\int_{-\infty}^{+\infty} \emptyset_k(z) \emptyset_{k'}(z)\, dz = \delta_{k,k'} \Delta z \quad (8c)$$

$$\int_{-\infty}^{+\infty} \emptyset_k \frac{\partial \emptyset_{k'+\frac{1}{2}}(z)}{\partial z} dz = \sum_{j=-L_s}^{L_s-1} a(j) \delta_{k+j,k'} \quad (8d)$$

$$a(j) = \frac{1}{\pi} \int_0^{\infty} \left|\widehat{\emptyset}(\lambda)\right|^2 \lambda \sin\lambda \left(j + \frac{1}{2}\right) d\lambda \quad (9)$$

The Fourier transform f (z) scaling function is represented by Φ^(λ).

Table. 1. Coefficients a(j) of Daubechies' scaling function (D4) [21]

j	Coefficient of a(j) for D_4
1	1.3110340773
2	-0.1560100110
3	0.0419957460
4	-0.0086543236
5	0.0008308695
6	0.0000108999
7	0.0000000041

Using the Galerkin approach [19] in equations (5a) and (5b) and the test functions $\Phi_k h_{n+1/2}(t)$ and $\Phi_{k+1/2}\, h_n(t)$, the following iterative computations for currents and voltages were performed:

$$I_{k+\frac{1}{2}}^{n+\frac{3}{2}} = B_1 I_{k+\frac{1}{2}}^{n+\frac{1}{2}} - \frac{\Delta t}{\Delta z} L^{-1} B_2 \left(\sum_{j=1}^{L_s} a(j) \left(V_{k+j}^{n+1} - V_{k-j+1}^{n+1} \right) \right) \quad (10a)$$

$$V_k^{n+1} = V_k^n - \frac{\Delta t}{\Delta z} C^{-1} \sum_{j=1}^{L_s} a(j) \left(I_{k+j-\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-j+\frac{1}{2}}^{n+\frac{1}{2}} \right) \quad (10b)$$

Where

$$B_1 = \left(1 + \frac{\Delta t}{2} R L^{-1}\right)^{-1} \left(1 + \frac{\Delta t}{2} R L^{-1}\right)$$

$$B_2 = \left(1 + \frac{\Delta t}{2} R L^{-1}\right)^{-1}$$

In order to update the iterative equations of currents and voltages and satisfy the connection coefficients a(j) provided by the connection coefficients a(j) given by, equations (10a) and (10b) must be decomposed using the relationship in [31].

$$\sum_{j=1}^{L_s} (2j-1) a(j) = 1 \quad (11)$$

Using (11) as a substitute in (10b), obtain

$$\sum_{j=1}^{L_s} (2j-1) a(j) V_k^{n+1} = \sum_{j=1}^{L_s} (2j-1) a(j) V_k^n - \sum_{j=1}^{L_s} \frac{\Delta t}{(2j-1)\Delta z} C^{-1} \left[(2j-1) a(j) \left(I_{k+j-\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-j+\frac{1}{2}}^{n+\frac{1}{2}} \right) \right] \quad (12)$$

Completing (10b) by taking into account the terms that correspond with j as follows:

$$(2j-1) a(j) V_k^{n+1} = (2j-1) a(j) V_k^n - (2j-1) a(j) \frac{\Delta t}{(2j-1)\Delta z} C^{-1} \left(I_{k+j-\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-j+\frac{1}{2}}^{n+\frac{1}{2}} \right) \quad (13)$$

for j=1, 2, 3, …., Ls

By using the at boundary conditions that are demonstrated in Sections 3.1 and 3.2, respectively, equation (13) is further modified.

3.1 Modeling with near-end boundary conditions:

The DIL system's modelling is applied with boundary conditions. The current and voltage nodes are at the near-end terminals designated by I_0 and V_1, respectively..

The nodal analysis of the terminal equation is given by:

$$V_s^n = R_d I_0 + V_1^n \tag{14}$$

At k =1,

$$V_1^{n+1} = V_1^n - \frac{\Delta t}{\Delta z} C^{-1} \sum_{j=1}^{L_s} a(j) \left(I_{j+\frac{1}{2}}^{n+\frac{1}{2}} - I_{-j+\frac{s}{2}}^{n+\frac{1}{2}} \right) \tag{15}$$

From the above equations (14) and (15), the iteratives equations at the near-end boundary nodes voltage of $V^{n+1}{}_1$ is obtained through the following:

$$V_1^{n+1} = V_1^n - \frac{\Delta t}{\Delta z} C^{-1} \sum_{j=1}^{L_s} 2a(j) \left(I_{j+\frac{1}{2}}^{n+\frac{1}{2}} - I_0^{n+\frac{1}{2}} \right) \tag{16}$$

In equation (16), by substitute $I_0^{n+\frac{1}{2}} = \frac{I_0^n + I_0^{n+1}}{2}$ and modifying equation (14) as $I_0 = \frac{V_s^n - V_1^n}{R_d}$ then obtained the equation (16) as

$$V_1^{n+1} = A_1 \left(A_2 V_1^n - R_d \sum_{j=1}^{L_s} 2a(j) I_{j+\frac{1}{2}}^{n+\frac{1}{2}} + \sum_{j=1}^{L_s} a(j)(V_s^{n+1} + V_s^n) \right) \tag{17}$$

where

$$A_1 = \left(CR_d \frac{\Delta z}{\Delta t} + \sum_{j=1}^{L_s} a(j) \right)^{-1}$$

$$A_2 = \left(CR_d \frac{\Delta z}{\Delta t} - \sum_{j=1}^{L_s} a(j) \right)$$

3.2 Modeling with far-end boundary conditions:

Similarly, the far-end terminal (k = NDZ+1) provides the nodal analysis equation at load current (I_{NDZ+1}) as follows:

$$I_{NDZ+1} = C_L \frac{dV_{NDZ+1}}{dt} \tag{18}$$

At the far end of the terminal, the final iterative equations are

$$V_{NDZ+1}^{n+1} = V_{NDZ+1}^{n} - D_1 D_2 \left(\sum_{j=1}^{L_s} a(j) I_{NDZ+1}^{n+\frac{1}{2}} - \sum_{j=1}^{L_s} 2a(j) I_{NDZ+1-j+\frac{1}{2}}^{n+\frac{1}{2}} \right) \quad (19)$$

Where

$$D_1 = \left(1 + C^{-1} \frac{C_L}{\Delta z} \sum_{j=1}^{L_s} a(j) \right)$$

$$D_2 = C^{-1} \frac{\Delta t}{\Delta z}$$

Thus, the MRTD iterative equations' stable output is known as the courant stability condition [22],[31].

$$\Delta t \leq \frac{q \Delta z}{v} \quad (20)$$

which specifies that the propagation time for each cell must be greater than the time step and q represents the current numbers provided by $q = 1/\sum_{j=1}^{L_s} |a(j)| = v\,\Delta t/\Delta z$ and v is the phase velocity of the line propagation.

4. MRTD Model Comparison and Validation:

For the measurement of the influence of line resistances on crosstalk peak voltage, delay analysis, the Driver-interconnects-load configuration is used. Via the proposed MRTD model, the parameters of a simulation are represented and validated. Identical linear driver resistive is used here to move the capacitive coupled interconnect lines and the bundled SWCNTs interconnects length is 2mm. The selection of structural characteristics occurs at the 32nm technology node. The load gate's input capacitance is 0.25fF, and the gate driver's equal output resistance and capacitance are 13.85kΩ and 0.07fF, respectively, denoted by Rd and Cout. Let R_{d_2} and R_{d_1}be the respective driver resistances for victim's and aggressor's lines.

The source voltages are meant to be for a ramp signal with a switching voltage of 1 V, and the sizes of the driver and the load are expected to be 100 times greater than the lowest gate sizes for interconnects. For all cases of crosstalk analysis, V_{s_1} and V_{s_2} are used a input's signals with a transitions time of 10ps and will fall from 1 to 0 and rise to a level of 0 to 1 V. Interconnects parasitic are tested for the bundled SWCNTs coupled transmission lines by selecting the physical parameters for the 32nm technology node [32].

$$R = \begin{bmatrix} 835.6 & 0 \\ 0 & 835.6 \end{bmatrix} k\Omega/\text{m}, L = \begin{bmatrix} 524.05 & 0 \\ 0 & 524.05 \end{bmatrix} nH/m, C = \begin{bmatrix} 9.65 & -5.79 \\ -5.79 & 9.65 \end{bmatrix} nF/m$$

In the MRTD analysis, 20 spatial discretizations (Nz) of transmissions lines with a line length of 2mm are considered, and the length of each section is equal to 0.1mm. The time step specifically follows the Courant stable condition and can be measured using a velocity (Vp) of 2.22 x 10^7 m/s. Temporal segments are calculated using the overall solution time divided by the time step. The voltages and currents of the transmission lines are obtained by using the MRTD model as set out in Section 3.

The caused delay can be accomplished by varying the line resistances from 200 to 2000kΩ/m to captures the effects on the crosstalk. The crosstalk induced delay is evaluated using the proposed model MRTD and FDTD method [32] and is correlated for both in-phase and out-phase switching cases with those obtained using SPICE tool, as seen in Figures 6 and 7. The findings show that the suggested MRTD model is in fair alignment with the SPICE simulation and significantly beats the FDTD model in terms of accuracy. Figures 6 and 7 demonstrate that as the line resistances increases, the in-phase's and out-phase's crosstalk induced delay increases, the out-phase crosstalk's induced delay is greater than the in-phase due to circumstance that the miller's capacitives effects doubles the capacitances of the coupling in the out-phase switching. The percentages of error in crosstalk caused delay are tabulated by the difference in line resistance in Table 2 and Table 3 for in-phase and out-phase switching's. It is noted that the FDTD method gives the percentages of an average error of 6.04 and 3.66, as the line resistances increases the crosstalk-induced delay increases, the suggested model gives the percentages of an average error of 2.96 and 1.86 for in-phase's and out-of-phase's switching, respectively with the effects of SPICE simulation. It is found that the percentage error decreases as the line resistances increases. The empirical results obtained using the model of MRTD are in strong alignment with the simulation of SPICE tool.

Table 2. Crosstalk induced delay due to variations in line resistances for in-phase switchings.

Line resistance (KΩ/m)	In-Phase Switching				
	SPICE (ps)	Proposed model (ps)	Duksh et al. model [32] (ps)	% error proposed model	% error [32]
200	2.76	2.62	2.57	5.0	6.9
400	2.77	2.63	2.58	5.0	6.7
600	2.77	2.66	2.59	3.9	6.5
800	2.78	2.68	2.60	3.5	6.4
1000	2.79	2.70	2.61	3.2	6.2
1200	2.79	2.71	2.62	2.8	6.2

1400	2.80	2.74	2.63	2.1	5.9
1600	2.81	2.75	2.65	2.1	5.5
1800	2.81	2.78	2.67	1.0	5.2
2000	2.82	2.79	2.68	1.0	4.9

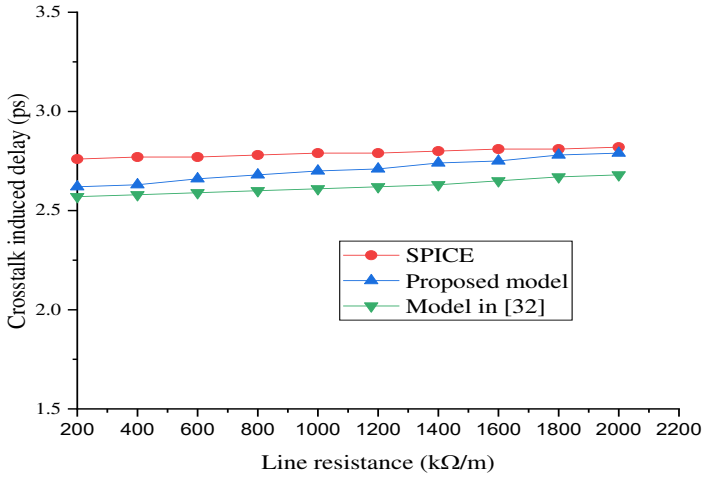

Figure6. Crosstalk induced delay due to line resistances for in-phase switching

Table 3. Crosstalk's induced delay due to variations in line resistances for out-phase switching.

Line resistance (KΩ/m)	Out-Phase Switching				
	SPICE (ps)	Proposed model (ps)	Duksh et al. model [32] (ps)	% error proposed model	% error [32]
200	4.37	4.20	4.17	3.8	4.6
400	4.38	4.23	4.18	3.4	4.5
600	4.39	4.27	4.19	2.7	4.6
800	4.40	4.30	4.21	2.2	4.3
1000	4.41	4.32	4.23	2.0	4.1
1200	4.42	4.36	4.26	1.3	3.7
1400	4.43	4.39	4.28	0.9	3.4
1600	4.44	4.40	4.32	0.9	2.8
1800	4.45	4.41	4.34	0.8	2.5
2000	4.46	4.43	4.37	0.6	2.1

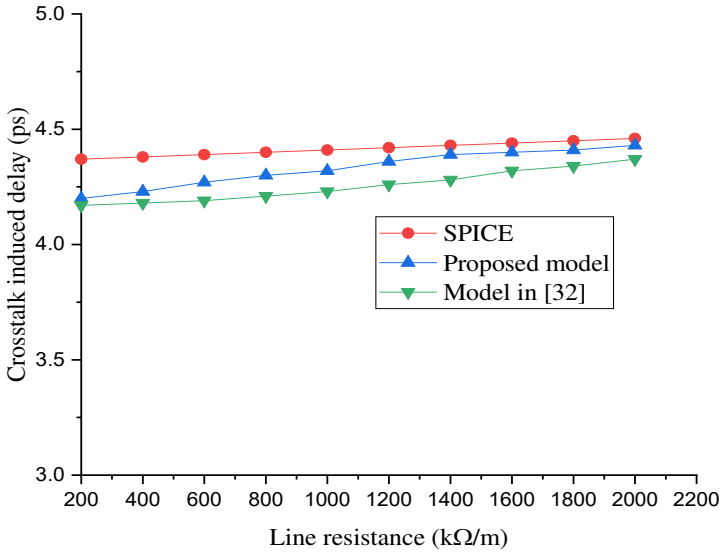

Figure7. Crosstalk induced delay due to line resistance variations for out-phase switching

Later, the line resistances is varied in order to trace its effect on the delay of propagation. Propagation's delay is obtained using the suggested MRTD model and the FDTD model is Compared to those that are obtained using SPICE and seen in Figure 8 for functional switching. The findings reveal that the suggested MRTD model is in strong alignment with the SPICE simulation and beats the FDTD approach in terms of accuracy. Figure 8 shows that as the in line resistance increase Propagation delay increases. The percentages of error in propagation delay are tabulated by varying the line resistances in table 4 for the functional. It is observed that as the in line resistances the propagation delay increases, FDTD method gives the percentages of an average error of 3.37, and the proposed model give's the percentages of average error of 1.78 for functional switching with respective to SPICE simulations results. It is also observed that as the in the line resistance increase the percentage error reduces. The empirical results produced with the MRTD model are highly consistent with the SPICE simulation.

Table 4. Propagation delay due to line resistance variations.

Line resistance (KΩ/m)	Propagation delay				
	SPICE (ps)	Proposed model (ps)	Duksh et al. model [32] (ps)	% error proposed model	% error [32]
200	3.49	3.38	3.36	3.1	3.7
400	3.50	3.39	3.36	3.1	3.9
600	3.50	3.40	3.37	2.8	3.8
800	3.51	3.42	3.38	2.5	3.7
1000	3.52	3.46	3.39	1.7	3.6
1200	3.53	3.49	3.41	1.1	3.4

1400	3.54	3.50	3.43	1.1	3.1
1600	3.55	3.51	3.44	1.1	3.0
1800	3.55	3.52	3.45	0.8	2.9
2000	3.56	3.54	3.47	0.5	2.6

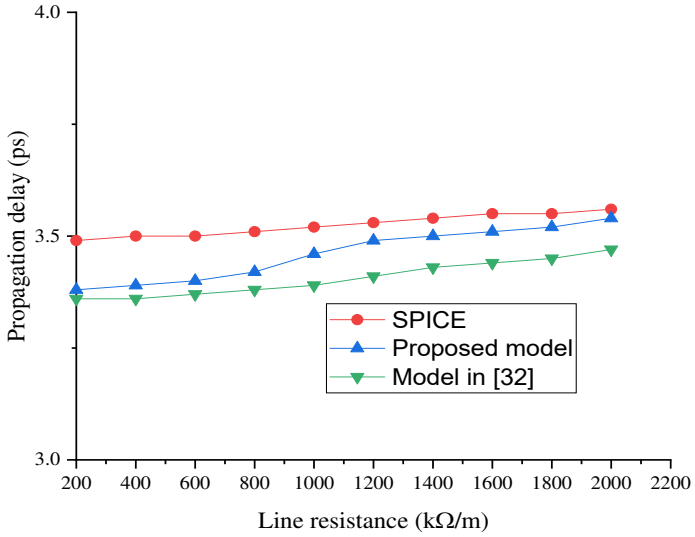

Figure 8. Propagation delay due to line resistance variations.

The peak voltages is observed under dynamics crosstalk and functional's crosstalk by varying the line resistances from 200 to 2000kΩ/m. Figure 9, indicates the peak voltages due to the effect of dynamic's crosstalk's of in-phase and out-phases switching conditions, which steadily decreases with an increases in line resistances. The peak voltage of the functional crosstalk remains constants for the higher values of the line resistances as seen in Figure 10. As the line resistances increases, the voltages steps along the line's differ with attenuation and dispersion. This is due to the facts that the voltages at the far end of the interconnect terminal is slightly lower than the voltages at the near ends. The percentages of the average error are to be less than 0.2 and 0.46 for the suggested MRTD and FDTD models respectively, in peak voltage, and therefore it can be concluded that the analyticals findings obtained using the MRTD techniques are in near alignment with SPICE tool simulations.

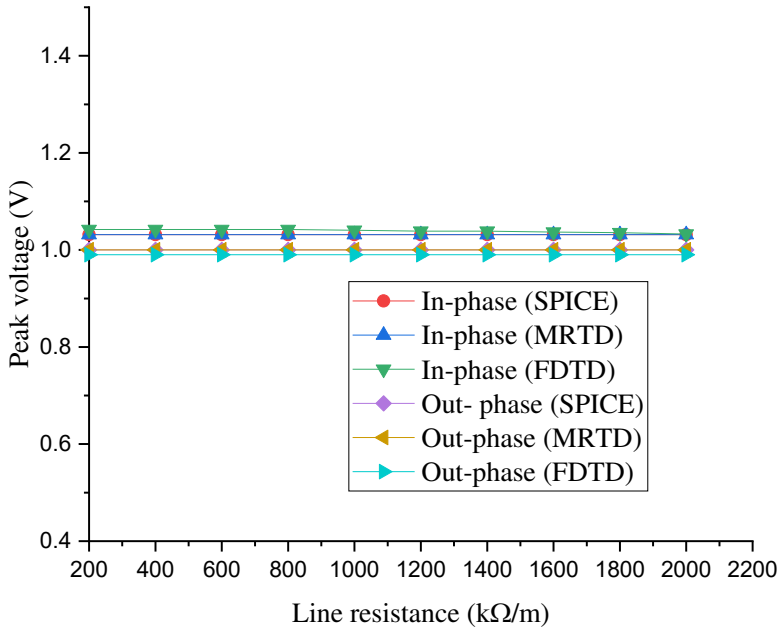

Figure9. Peak voltages due to line resistance variations for dynamic crosstalk.

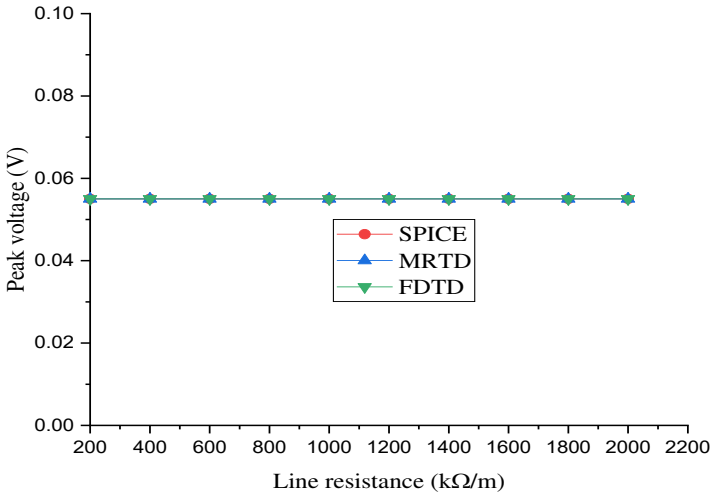

Figure10.Peak voltage due line resistance variations for functional crosstalk.

5. Conclusion:

This paper is based on the MRTD model for functional crosstalk and dynamic crosstalks analysis of coupled transmission lines driven by linear resistance. The most effectives time domain analysis is presented for coupled transmissions lines built on SWCNT bundle interconnect. The proposed model specifically assumes the condition of the courant stability condition. The effects of line resistances on crosstalk effects were evaluated for delay measurement, while out-phase, in-phase and functional crosstalk and also the estimated noise peak voltages. Comparisons are made between the FDTD and SPICE simulations and the empirical results obtained with the MRTD model. The results obtained using the proposed MRTD model reveal that the average errors is estimated to be less than 2.96% and 1.86% for in-phase and out-phase crosstalk induced delays, 1.78% for functional propagation delay. In addition, it is also

observed that the peak voltages under functional and dynamic crosstalk has an average error of less than 1% relative to SPICE simulations. The proposed MRTD model's great accuracy and strong agreement with the SPICE tool are confirmed by the FDTD for SPICE and the MRTD model itself. The research was performed on capacitive-coupled interconnects, but it is also applicable to CMOS-driven and mutually coupled interconnects.

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