Scope

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Design of a Low Noise Figure Lnausing a Novel Coupled Inductor

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Abstract:

Problem: A low noise amplifier (LNA) design requires minimum noise introduced by the amplifier. This can be achieved by reducing the losses at the LNA's input and matching the LNA's input noise impedance with the source impedance. On-chip inductors generally have higher losses due to lower-quality factors, and this affects the noise performance of the on-chip LNAs. **Approach:** The paper presents a novel pyramid and coupled pyramid inductor to improve the quality factor. The improvement in quality factor is achieved by reducing the parasitic capacitance and losses utilizing a multilayer structure and also by varying the length of the inductor in each layer. The coupled pyramid inductor is designed using Sonnet software. **Findings:**The pyramid and coupled inductors achieve a quality factor of 16.8 and 17.15. The inductance values for these inductors are 1.92 nH and 4.85 nH, respectively. The effect of the quality factor and the inductance are validated by designing a low noise amplifier at 5.5 GHz. The LNA's simulated noise figure and gain are 1.09 dB and 15.6 dB. **Conclusion:**The losses in the coupled inductor are decreased by reducing the width of the conductor at each layer to compensate for the eddy currents and also the substrate losses. This results in the improvement of the inductance and quality factor in the coupled pyramid inductor. The reduced losses result in improved LNA performance, which can be observed from the Figure of Merit (FoM) of 14.6 for the LNA.

Keywords:current crowding effect, low noise amplifier (LNA), Spiral inductor, noise figure, quality factor.

1. Introduction

Inductors are widely used in many applications like filters, matching network, Phase Locked Loop (PLL), and tuning circuits, which require high-quality factors at high frequencies [1]. Designing high-quality factor on-chipinductors with high inductance values is still a highly challenging task. The quality factor of the on-chip inductor will be limited mainly due to substrate loss, resistive loss, and eddy current loss [2, 3]. The quality factor and inductance of on-chip inductors are affected by the variation in conductor width, spacing between conductors, and the number of turns [4].

Several techniques have been employed to improve the performance of the inductors, such as using different geometries, shielding, stacking layout techniques, loss reduction techniques, etc. [5]. The inductor's size and shape impact the quality factor, and circular inductor and octagonal inductors provide the best quality factor due to their small footprint and lower substrate losses. Coupling among the metallic strips of the inductor reduces the quality factor and the self-resonant frequency. A patterned ground structure is used to overcome this, which provides the shielding effect, reducing the capacitance to ground, conductive loss of the metal track, and dielectric loss of the substrate [6]. It also reduces turns number for the inductor due to the shielding effect. Parasitic capacitance in inductors reduces the self-resonant frequency and degrades the performance of the inductors when used in LNA applications. A high inductance inductor can be achieved in stack inductor design due to the self-inductance and mutual inductance of the structure [7]. Taper structure is employed to enhance the quality factor in stacked inductors [8]. The taper structure reduces the eddy current, and the varying line width and spacing dimensions increase the stored energy and hence the quality factor. Another parameter that reduces the quality factor is the current crowding effect, and this can be reduced by designing the inductors to carry current in multi-paths [9]. The current flowing in opposite paths produces opposing magnetic fields, reducing current crowding and enhancing the quality factor. However, the multi-path methodmay not always be useful as the inner paths are shorter and the outer paths are larger [10]. Metal stacking can be utilized to improve the quality factor. The two twisted loops produce magnetic fields of equal magnitude and opposite polarities, reducingthe current crowding effect and enhancing the quality factor.

Low noise amplifiers have been designed in various topologies and technologies. A three-stage cascade LNA is designed with a gain of 38 dB and a noise figure of 2.4dB for IoT applications [1]. The LNA adopts reactive adaption architecture for its design to increase the gain.A common gate cascade LNA using resistive load is designed to reduce the chip size. The LNA achieves better than 20 dB gain, and noise figure less than 3dB. An inductor-less LNA has been designed employing a noise cancellation technique [13]. The LNA achieves a gain of 19 dB and a noise figure of 3.4 dB with a power dissipation of 8.4mW. A common gate LNA is presented for LTE application at 2.6 GHz in Ref. [14]. Gm-boosted configuration is used for the LNA to achieve a lower noise figure, and a notch filter at the input is used for the impedance matching. The LNA delivers a 20 dB gain and a minimum noise figure of 2.6dB.

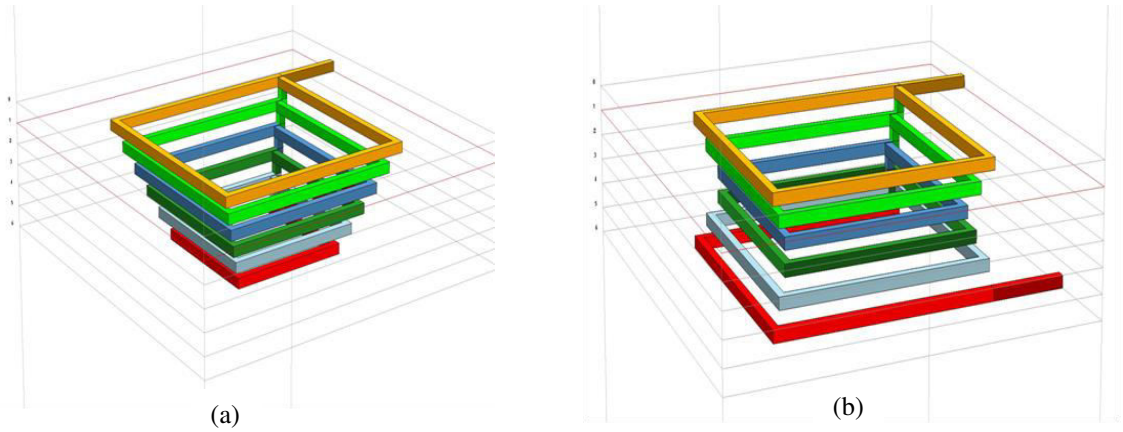
This paper proposes a novel pyramid and coupled pyramid inductor in a multilayer configuration. The structure reduces the interlayer capacitance and eddy current, increasing the inductance and quality factor, respectively. The effect of quality factor and losses is demonstrated by designing a low noise amplifier with the coupled inductor as a matching element. The designed single-stage LNA achieves a noise figure and gain of 1.09 dB and 15.6 dB, respectively. The paperdescribes the proposed novel structure in Section II. The pyramid and coupled pyramid inductor analysis and simulation results are discussed in section III. Section IV deals with the simulation of anLNA with the coupled pyramid inductor. Section V presents the conclusion.

2. Proposed Multilayer Inductor Structure

Calculation of inductance is critical in the design of an on-chip inductor. The total inductance can be calculated as series inductance of individual conductors and mutual inductance. When the current is carried in the same direction, then the positive coupling is increased, and inductance increases when in two metal tracks, currents are flowing in opposite directions, and they are placed close to each other. The overall inductance decreases. The effect of self and mutual inductance on the overall DC inductance of the inductor is discussed in [3].

The proposed inductor is designed to improve the quality factor and inductance. The pyramid inductor is designed such that the inner diameter is varied from topto bottom layer.As the layer increases, the inner diameter decreases by 2um.To improve the inductance, two turns are taken at each layer, and in every layer, variable width and dimension are taken to increase the quality factor of the proposed inductor, as shown in Fig. 1(a).The pyramid inductor is designed with a conductor width of 2 um, the spacing between the conductor is 0.5um, and the thickness of the conductor is 2um. The outer diameter of the inductor is reduced as the inductor is designed in the lower metal layers. This reduces the field coupling between the adjacent layers and improves the substrate losses due to field coupling and displacement current.

The coupled pyramidal inductor is designed similarly to the pyramid inductor as shown in Fig. 1(b); however, in this case, the outer diameter is reduced to three bottom layers and then increased symmetrically for the next three layers. The stacked structure further reduces the substrate loss and field coupling,increasingthe inductance and quality factor. The width of the conductor is 2um, the gap between the conductors is 0.5um, and the thickness of the conductor is 2um.Stacking the metal strips symmetrically reduces the eddy current loss and crowding effect by reducing the magnetic fields entering the substrate.



(a) (b)

Fig. 1 (a) Pyramidinductor(b) Coupled pyramid inductor

3. Simulated Results of Pyramid and Coupled Pyramid Inductor Structure

To verify the simulation results of the proposed inductor, SONNET simulation tool is used for the EM simulation. Silicon substrate with 100um thickness is used for the design of the inductor. The parameters of the proposed inductor are calculated using eq. (1-3) from the Y parameters. These Y-parameters are converted from S-parameters.

$$L = \frac{1}{2\pi f}\,\mathrm{Im}\left[\frac{1}{Y_{11}}\right] \tag{1}$$

$$Q = -\frac{\mathrm{Im}\left[\frac{1}{Y_{11}}\right]}{\mathrm{Re}\left[Y_{11}\right]} \tag{2}$$

$$R_s = \frac{1}{\mathrm{Re}\left[Y_{12}\right]} \tag{3}$$

The above parameters are shown in Fig. 2 and Fig. 3. The coupled inductor has an improved inductance value over the pyramid inductor, as observed in Fig. 2. The quality factor improvement is marginal. However, the higher inductance value is usual for the design of inductors at lower frequencies. A compact inductor can be used for obtaining a higher value of inductance using a coupled inductor. Table 1 compares the performance of the pyramid and coupled pyramid inductor.

Table 1 Comparison of pyramid and coupled pyramid inductor

Parameters	Pyramid	Coupled pyramid
Inductance (nH)	1.92	4.85
Peak quality factor	16.8	17.15

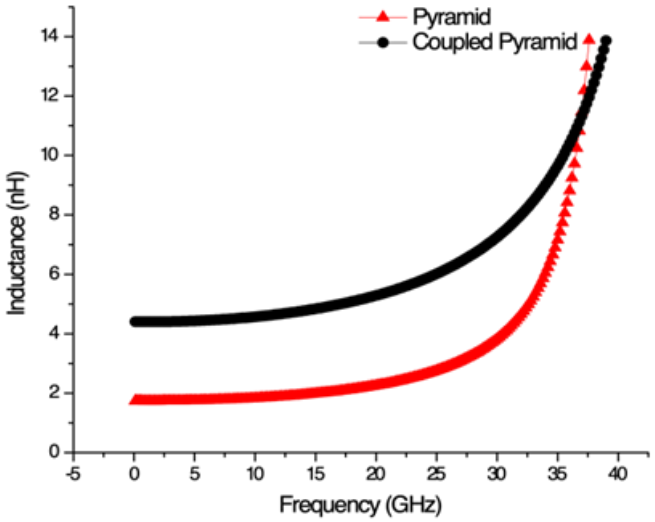


Fig. 2 Comparison of the inductance of pyramid and coupled pyramid inductor

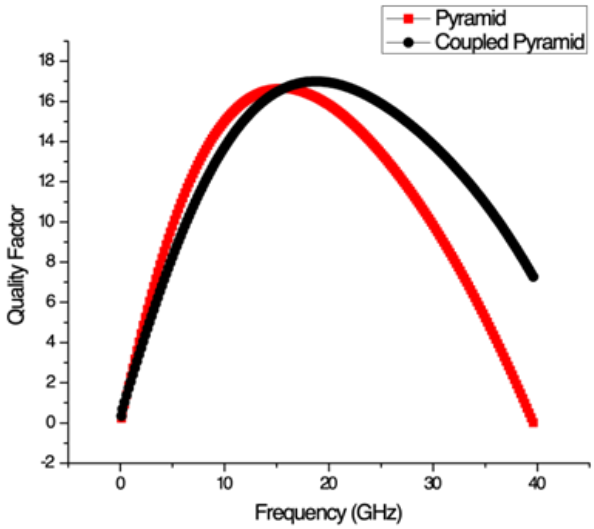


Fig. 3 Comparison of the quality factor of pyramid and coupled pyramid

4. Design of a Low noise amplifier with a Coupled Pyramid Inductor Structure

The designed inductor finds applications in amplifiers, VCOs, and filters. In this paper, the performance of the coupled inductor is assessed by using it in the input noise-matching network of LNA. The basic amplifier is designed in a common emitter inductive degeneration configuration. The amplifier is noise-matched at the input using a shunt inductance and series capacitance, as shown in Fig. 4. The series capacitance also serves as a blocking capacitor to avoid DC leakage. The biasing circuit for the amplifier consists of a lowpass filter and current-controlling resistors. The low pass filter for the base bias consists of a shunt capacitor, and the drain bias consists of a parallel tank circuit, shunt capacitor, and current-controlling resistors. The output matching has been achieved using an L network consisting of a shunt capacitor and a series inductor for power matching. The transistor is unstable for operation frequencies; hence, shunt inductances are used to stabilize the transistor,, and two inductors are used to reduce the parasitic resistance. This negative feedback resistance reduces the gain of the amplifier. The optimized values of the various components discussed above for the common emitter amplifier are shown in Fig. 4. The amplifier circuit is analyzed using S-parameters to measure the gain, input return loss, noise figure, and stability.

In Fig.5, the S-parameters of the LNA with the proposed inductor are compared with the LNA's S-parameters designed with an inductor having a quality factor of 5. The proposed inductor and inductor with quality factor 5 are represented as CPI and Q5, respectively. The single-stage LNA provides a gain in excess of 15 dB (S21) with input (S11) and output return loss (S22) better than 10dB. The isolation between the output and input ports is better than 20dB. The gain and isolation of the proposed inductor is 0.5 dB better than the inductor with a quality factor 5. This is due to the insertion loss of the inductor.

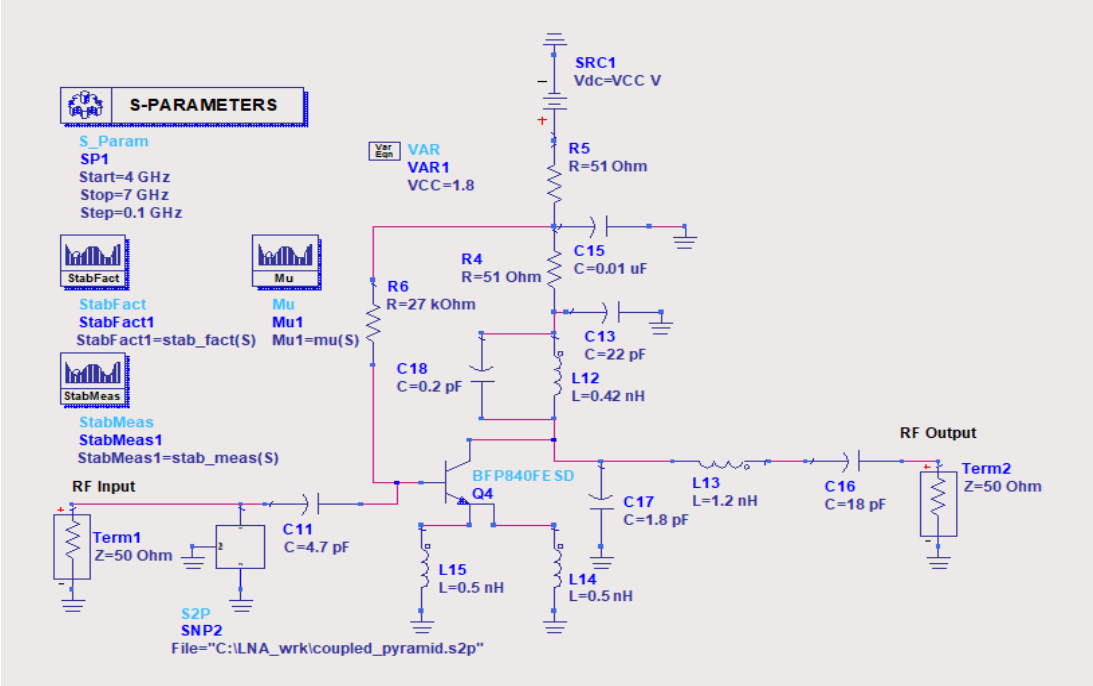


Fig. 4 The LNAschematic simulation.

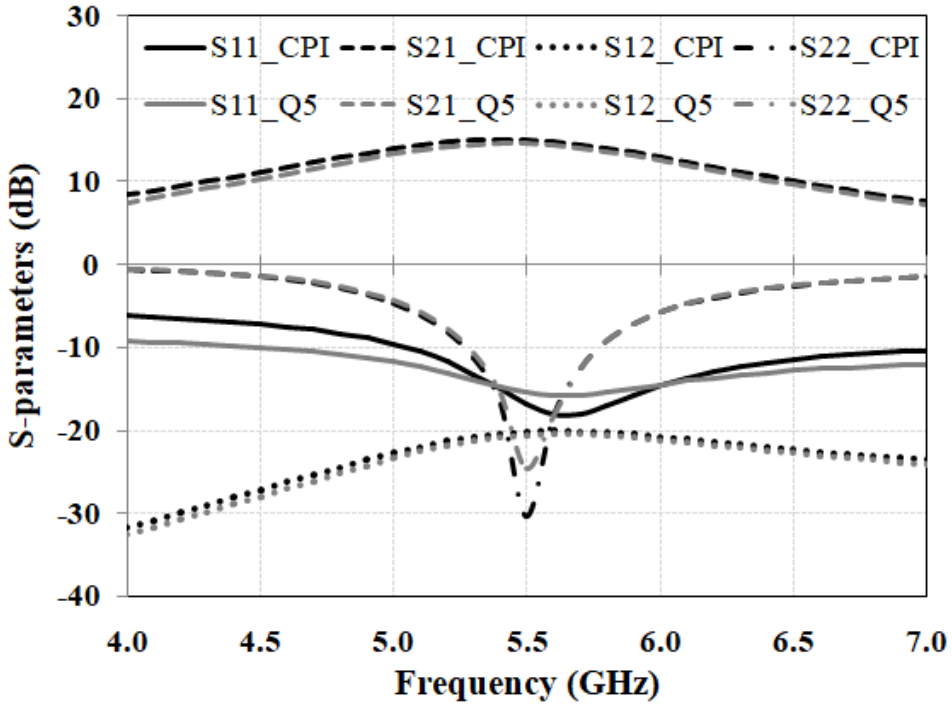


Fig. 5S-Parameters of the LNA

The gain of the LNA can be tuned further, but the noise figure would degrade. The simulated noise figure of the LNA is shown in Fig. 6. The noise figure of the LNA due to the proposed inductor is 1.09 dB, and that of the inductor with quality factor 5 is 1.65 dB at 5.5 GHz. This increase in the noise figure is due to the quality factor and losses associated with the inductor. This substantiates the effectiveness of the proposed inductor with respect to quality factors.

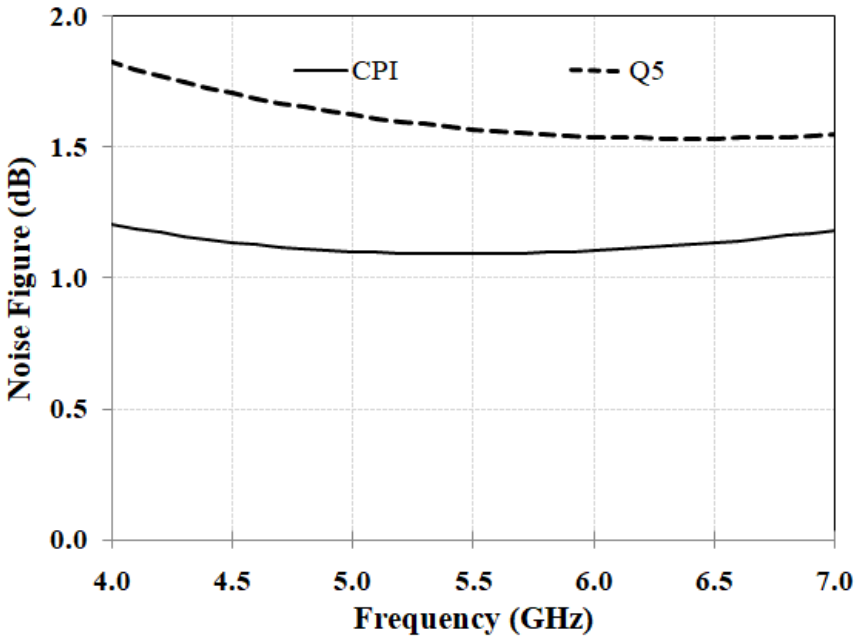


Fig. 6VCO output frequency variation over the Varactor capacitance

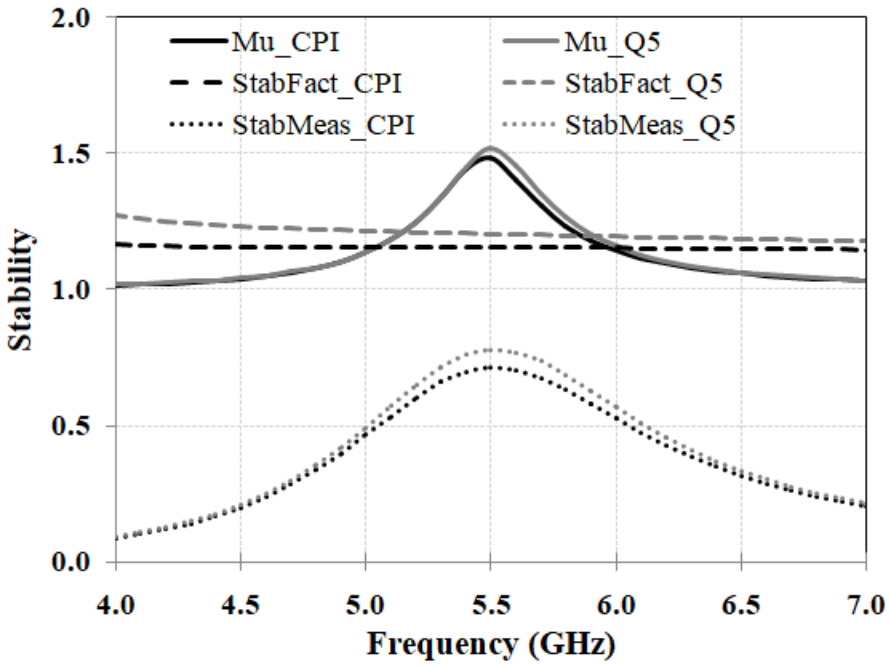


Fig. 7Output power over the frequency band of VCO

The stability factor of the LNA with the two inductors is shown in Fig. 7. The LNA is stable with both inductors. The performance of the LNA can be estimated using a figure of merit (FOM) given by eq. (4) [11]

$$FOM = \frac{G.F_0}{(NF_{\min} - 1) * P_D} \quad (4)$$

Where G is the gain of the LNA, F_0 is the centre frequency in GHz, NF_{min} is the minimum noise figure value, and P_D is the power dissipated by the LNA in milli-Watts. Table 2 compares the FOM of the proposed LNA with other recently published LNAs.

Table 2 Comparison of LNA parameters

Parameters	[1]	[11]	[12]	[13]	[14]	This works
Centre Frequency (GHz)	10	2.15	2.4	4.6	2.6	5.5
Gain (dB)	11	22	20	19.2	20.9	15.6
Noise Figure (dB)	1.9	2.4	3.9	3.1	2.6	1.09
Power dissipation (mW)	50	5	2	8.5	5.76	5.5
FOM	1.13	7.8	9.5	3.7	6.2	14.6

The noise figure of the proposed LNA is 1.09 dB, the lowest, and the FOM is the best among the references. The gain of the proposed LNA is lower due to single-stage configurations, whereas the other references are designed in cascade or cascade configuration. The figure of merit for the LNA combines all the important parameters and provides a good measure of the performance of the LNA. The proposed LNA has a FOM of 14.6.

5. Conclusion

In this paper, a pyramidal inductor is designed and subsequently modified to a coupled pyramid inductor in multilayer technology. The coupled inductor width is decreased at each layer to compensate for the eddy currents and substrate losses. The inductance and quality factor improvement is observed in the coupled pyramid inductor. The inductor's performance is validated by designing the input matching circuit in LNA design. The LNA exhibits a noise figure of 1.09 dB and a gain of 15.6 dB at 5.5 GHz. The coupled pyramid inductor is best suited for the design of filters, amplifiers, oscillators, and receiver circuits for various communication applications.

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