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Simulation of Double Gate TFET With Different Gate Oxides and Thickness

Chinnala. Pavan Kumar [1] **K.Sivani**[2]
Kakatiya Institute of Technology & Science Warangal, Telangana state, India

Corresponding author. E-mail: chpk.ece@kitsw.ac.in

Abstract: Transistors have changed the world. Everyday our world is progressing by making the electronic devices faster and efficient. Transistors are of two types they are BJT's and FET's. FET's are used for their extensive advantages over BJT[1]. MOSFET's are well known for their switching speed but compare to MOSFET tunnel FET has many advantages as it provides more switching speed and it performance well with low power applications and low threshold voltage this makes tunnel FET (TFET) popular over MOSFET. Due to increase in power density it is difficult to continue MOSFET scaling due to sub-threshold swing (SS). One of the best choices to replace the MOSFET for the applications of low power is the TFET[4]. The operation of TFET, it works on the concept of band-to-band tunnelling (BTBT) of electrons. Double gate tunnel field effect transistor overcomes the limitations of leakage current and sub-threshold slope but it also has a drawback of ambipolar behaviour due to its symmetrical source drain architecture, the solution for this is to introduce some asymmetry between source and drain this is through the step channel thickness[3]. The more band-to-band tunnelling of electronics from source to channel it leads to more enhancement in on state current. In this paper different gate oxides, Thickness of oxide are tested, the simulation of double gate tunnel FET will be performed by using cadence software.
Keywords: TFET, MOSFET, DG-TFET,P-I-N TFET

I. Introduction

Tunnel FET are gated P-I-N diodes, where on state current arises from band to band tunneling, are more attractive new device structures for ultra-low power applications because of their low off state current[2]. Due to P-I-N body of the TFET it also eliminates latch-up internally unlike MOSFET Double gated tunnel field effect transistor overcomes the limitations of leakage current & sub-threshold slope (SS) but it also has a drawback of ambipolarity due to its symmetrical source drain architecture, the solution for this is to introduce some asymmetry between source and drain this is through the step channel thickness.

Since DG-FETs provide better performance at lower supply voltages than MOSFETs, they are becoming a promising alternative to conventional MOSFETs. Understanding how these elements impact device performance can be done by simulating DG-TFETs with various gate oxides and thicknesses. The gate capacitance, which in turn impacts the switching speed and power consumption of the device, is heavily influenced by gate oxide thickness. The choice of gate oxide material can impact the overall performance of the device.

These simulations can provide valuable information on parameters such as the sub threshold slope, drain current and transconductance, which are key parameters for TFETs. One of the best choices to replace the MOSFET for the applications of low power is the TFET[2]. The operation of tunnel field effect transistors works on the principle of band-to-band tunnelling (BTBT) of electrons[3]. Double gate tunnel field effect transistor overcomes the limitations of leakage current and sub-threshold slope but it also has a drawback of ambipolar behaviour due to its symmetrical source drain architecture, the solution for this is to introduce some asymmetry between source and drain this is through the step channel thickness.

II. Proposed and Existing Methods

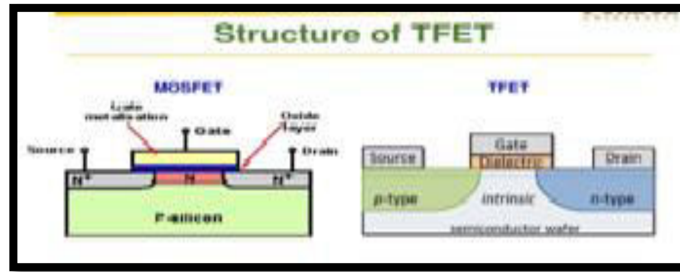

Fig 1: Structure of TFET

The above is the figure of tunnel FET. The tunneling will takes place between the intrinsic and a P+ regions. Positive bias is applied to drain terminal & a source terminal is grounded without gate voltage, then the width of energy barriers between the intrinsic & a P+ region is very high, it is around 10nm. In this state the device is in off state[7]. As of Vg increases the barrier decreases, narrowing tunnel barriers allowing tunneling current to flow Voltage swing; is evaluated between the voltage at which current starts to increase with the increasing gate-voltage & threshold voltage.

A MOSFET had constant slope between off-state & threshold. A TFET develops a slope that is steeper. TFET voltage swing is less compared to MOSFET. As a result, when compared with MOSFET the current had exponential dependence on square root of the gate capacitance. Based on this we are focused on device optimization.

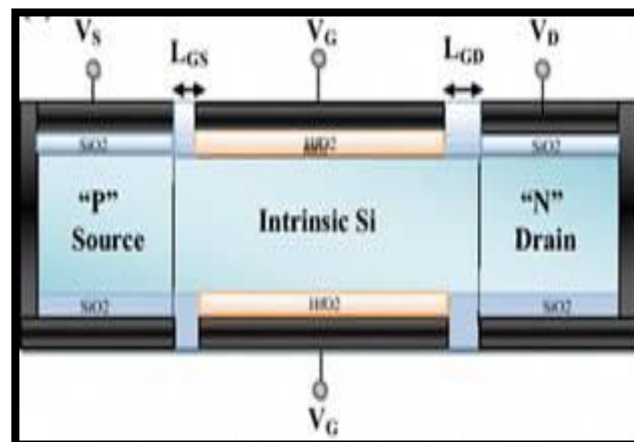

Fig 2: Structure of DG-TFET

The advantage of the extra gate in the TFET is that it doubles the current. As a result, the inrush current is amplified and the turn-off current is femtoampere or picoampere[4]. Using a high-k subthreshold dielectric swing also reduces the swing, making it very efficient.

III. .Study of Transfer Characteristics

A. Transfer Charecteristics

A drain source voltage of 5 volts is applied to obtain the transfer characteristics i.e Ids Vs Vgs for the proposed device with a gate oxide 22(tantalum pentoxide) and thickness of oxide 2.3um. We obtain Ids of 0.7mA at Vgs of -1 volts.

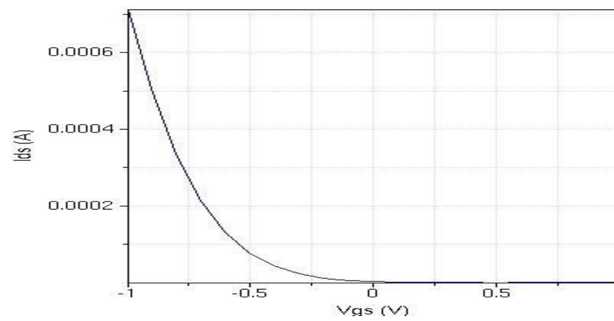

Fig 3: Drain current Vs Gate voltage at 2.3um

For the same drain source voltage for the proposed device with a gate oxide 22(tantalum pentoxide) and thickness of oxide 2um We obtain a better output drain current of 0.82mA at Vgs of -1 volts.

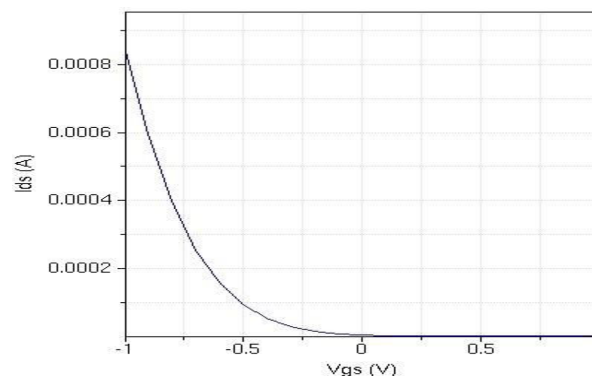

Fig 4: Drain current Vs Gate voltage at 2um

For the same drain source voltage for the proposed device with a gate oxide 22(tantalum pentoxide) and thickness of oxide 1um We obtain a better output drain current of 1.62mA at Vgs of -1 volts.

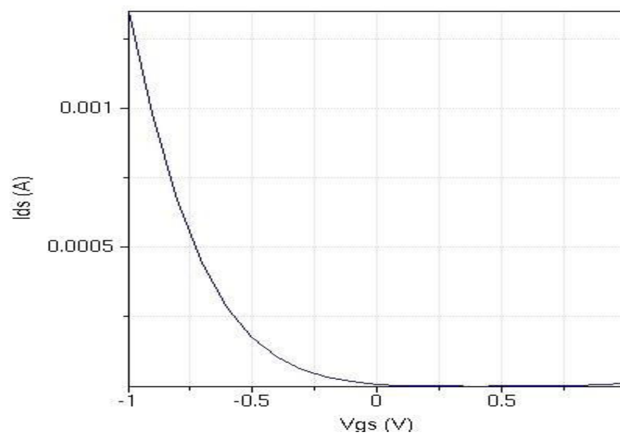

Fig 5: Drain current Vs Gate voltage at 1um

A drain source voltage of 5 volts is applied to obtain the transfer characteristics i.e Ids Vs Vgs for the proposed device with a gate oxide 25(Zirconium dioxide) and thickness of oxide 2.3um. We obtain Ids of 0.826mA at Vgs of -1 volts.

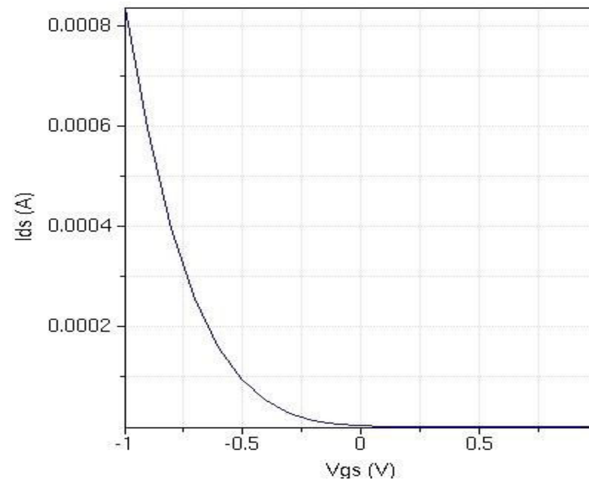

Fig 6: I_{ds} Drain current Vs V_{gs} Gate voltage at 2.3um

For the same drain source voltage for the proposed device with a gate oxide 25(Zirconium dioxide) and thickness of oxide 2um We obtain a better output drain current of 0.95mA at Gate voltage (Vgs) of -1 volts.

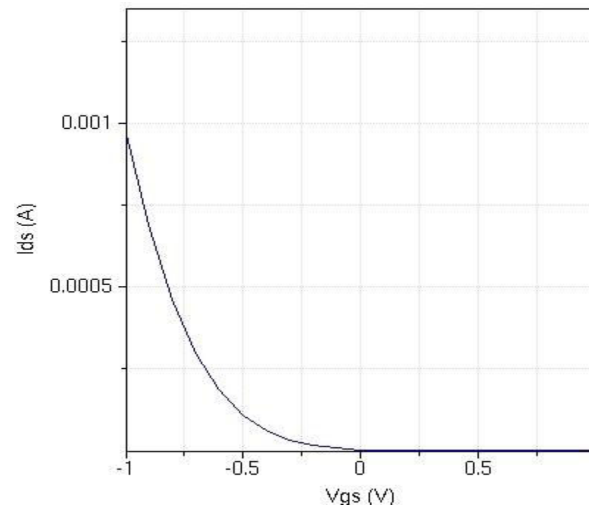

Fig 7: Drain current Vs Gate voltage at 2um

For the same drain source voltage for the proposed device with a gate oxide 25(Zirconium dioxide) and thickness of oxide 1um We obtain a better output drain current of 1.96mA at Gate voltage (Vgs) of -1 volts.

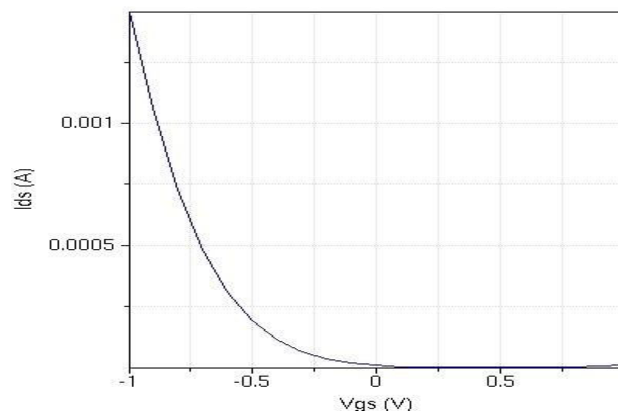

Fig 8: Drain current Vs Gate voltage at 1um

OBSERVATIONS RECORDED IN TABLE (TRANSFER CHARACTERISTICS)

Gate oxide(esp_ox)	Vgs	tox	Ids
22(Tantalum pentaoxide)	-1v	2.3um	0.7mA
		2um	0.82mA
		1um	1.62mA
25(Zirconium dioxide)	-1v	2.3um	0.82mA
		2um	0.95mA
		1um	1.96mA

IV. STUDY OF OUTPUT CHARECTERISTICS

A. *OUTPUT CHARECTERISTICS*

A gate voltage of 1volt is applied to obtain output characteristics i.e I_{ds} Vs V_{ds} for proposed device with a gate oxide 22(tantalum pentoxide) and thickness of oxide 2um. We obtain the drain current 1.41319e-08A at drain source voltage (Vds) of 1.9 volts.

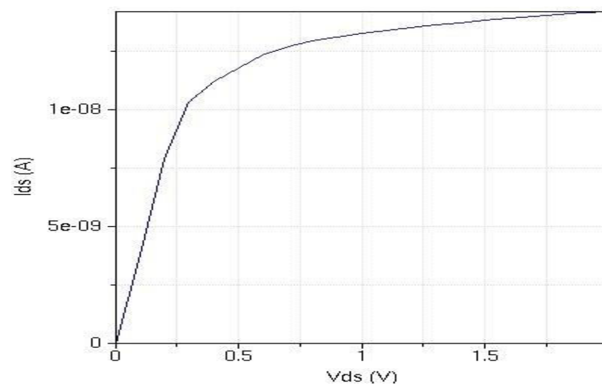

Fig 9: I_{ds} Drain current Vs V_{ds} Drain Source voltage at 2um

For the same gate voltage for the proposed device with a gate oxide 22(tantalum pentoxide) and thickness of oxide 1um We obtain a better output drain current of 1.92e-07A at drain source voltage (Vds) of 1.9 volts.

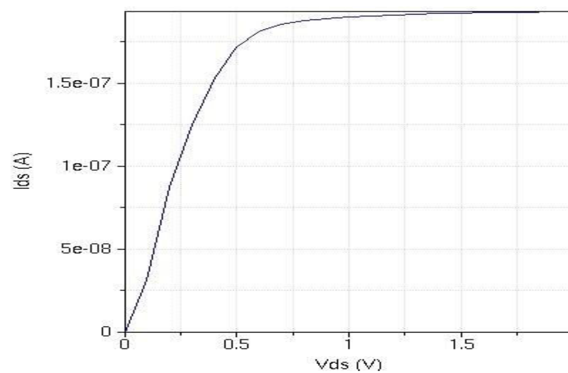

Fig 10: I_{ds} Drain current Vs V_{ds} Drain Source voltage at 1um

A gate voltage of 1 volts is applied to obtain output characteristics i.e I_{ds} Vs V_{ds} for proposed device with a gate oxide 25(Zirconium dioxide) and thickness of oxide 2um. We obtain the drain current 2.46193e-08A at drain source voltage (Vds) of 1.9 volts.

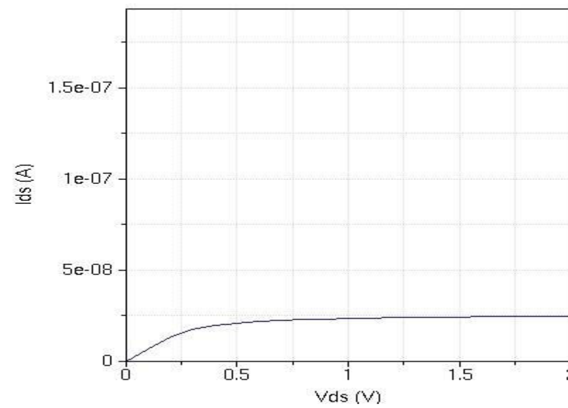

Fig 11: Ids Drain current Vs Vds Drain Source voltage at 2um

For the same gate voltage for the proposed device with a gate oxide 25(Zirconium dioxide) and thickness of oxide 1um. We obtain a better output drain current of 2.64601e-07A at drain source voltage (Vds) of 1.9 volts.

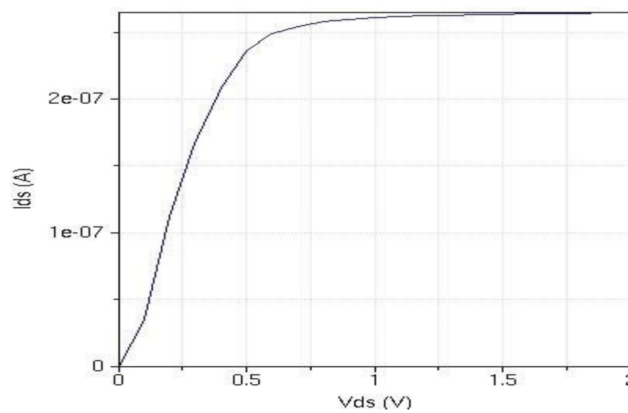

Fig 12: I_{ds} Drain current Vs V_{ds} Drain Source voltage at 1um

OBSERVATIONS RECORDED IN TABLE (OUTPUT CHARATERISTICS)

Gate oxide(esp_ox)	Vds	tox	Ids
ılum pentaoxide)	1.9v	2um	1.41319e-08A
		1um	1.92e-07A
25(Zirconium dioxide)	1.9v	2um	2.46193e-08A
		1um	2.64601e-07A

The tantalum pentoxide (Ta2O5)has high-k dielectric material, like zirconium dioxide (ZrO2), which means that it has a higher dielectric constant than customary silicon dioxide (SiO2) gate oxides.In addition to having high-k characteristics, Ta2O5 also has a sizable bandgap and a strong breakdown electric field. Ta2O5 can be used to lower the device's threshold voltage, which will enhance on-current performance.

Due to its high dielectric constant compared to tantalum pentoxide zirconium dioxide (ZrO2) is frequently used in double-gate Tunnel Field Effect Transistor (TFET) simulation with various gate oxides and thicknesses. This can help to lower the device's gate leakage current and increase its on/off current ratio. Furthermore, the relatively high bandgap of ZrO2 can aid in minimising the effects of tunnelling current through the gate oxide.

Due to its high dielectric constant, low bandgap, and compatibility with conventional semiconductor processing methods, ZrO2 is an ideal material for use in double-gate TFET simulations. Due to these characteristics, it is an excellent choice for use in the gate oxide layers of double-gate TFET devices, where it can enhance their performance.

V. Results

The final results obtained from above observations are:

1. The relation between Thickness of oxide (tox) and Drain current (Ids) is given by:
   Tox ∝ 1/Ids
2. The relation between Drain current (Ids) and Gate voltage (Vgs) is given by:
   Vgs ∝ 1/Ids

Hence by using Zirconium dioxide with 1um thickness, more enhancement in I_{ds} is observed.

VI. CONCLUSION

The double-gate tunnel field-effect transistor (DGTFET) is a promising device for low-power applications due to its steep subthreshold swing and low off-state current. The thickness and material of the gate oxide in DGTFETs play a crucial role in determining the device's performance. Studieshave shown that using different gate oxide thicknesses in DGTFETs can significantly affect their electrical characteristics. A thinner gate oxide results in a higher tunnelling current, while a thicker gate oxide leads to a higher gate capacitance and a lower subthreshold swing.

Additionally, using different gate oxide materials can also affect the device's performance. For example, silicon dioxide (SiO2) gate oxides have been found to exhibit a higher tunnelling current than other materials such as high-k dielectrics.In conclusion, the choice of gate oxide thickness and material in DGTFETs can have a significant impact on their performance. Further research in this area may lead to the development of more efficient and low-power devices for future electronics applications.

Statements & Declarations

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Competing Interests

"We have no relevant financial or non-financial interests to disclose."

Author Contributions

All authors read and approved the final manuscript.

Data Availability

"The results generated or analysed during the current study are available in the [Heterojunction tunnel field-effect transistor suitable for high-speed low-power applications] repository,

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