Design 4: 1 Multiplexer Using GDI (90 NM) Technology for Low Power and Compact Area

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Abstract: The multiplexers (MUXs) are essential combinational circuits widely used in digital systems for data selection and routing. This work presents the design and execution of a 4×1 multiplexer using a hierarchical approach based on 2×1 multiplexers, implemented with the Gate Diffusion Input (GDI) technique. The GDI technique allows substantial transistor count reduction in comparison to traditional CMOS logic, leading to lower power usage as well as smaller silicon area. Also, the technique archives higher speed and is energy efficient. In the suggested architecture, multiple 2×1 MUX modules are interconnected to realize the 4×1 MUX functionality, leveraging the GDI's ability to implement complex logic functions with reduced area. The design is implemented on 90 nm technology. Performance metrics like power dissipation and area were analysed and compared with conventional CMOS. Simulation results demonstrate that the proposed GDI-based 4×1 MUX achieves the reduction in total power consumption (51.4%), area (48.6%), improvements in speed and energy efficiency, making it suitable for use in low-power and high-performance digital circuits.

Keywords: Multiplexer, CMOS, GDI, Cadence tool

1. Introduction

Advances According to Moore's law, integrated circuit transistor counts double every two years. [1]. By increasing the quantity of IC transistors, the power consumption is reduced. The need for low-power devices has led to a major shift in standards, and power dissipation is now a major consideration regarding performance and [2]. In the contemporary hardware industry, low power has become a matter of concern.

A circuit that combines one output and several inputs, the multiplexer selects one line from a number of them and sends data to the single output line via information lines. Another name for an information selector is what the multiplexer is [3]. A multiplexer with a 4:1 ratio is a fundamental "switch logic" arrangement. The switch logic is created using variety of switches rather than utilizing gates. There are various design stages that can satisfy the growing need for very large-scale integration with low power usage (VLSI), including the

circuit and layout, architectural, and the level of technology for processes [14]. Selecting right logic style for the implementation of the combinational circuit provides a significant saving of power at the circuit design level. This is due to the fact that the logic style used has a significant impact on all of the crucial factors controlling short-circuit currents, transition activity, switching capacitance, and power dissipation. Different performance factors become significant based on the intended use, the kind of circuit that will be used, and the process of design employed in making it. Through the use of gate diffusion input technique, pass transistor logic, dual pass transistor logic types, complementary CMOS, and transmission gates, this study examines a 4-to-1 multiplexer for the number of transistors, power use, and delay to compare the implementations.

The multiplexer transmits the chosen entry into a single line. Another term for an input multiplexer is a data selector, which includes 'n' choose phrases that are used to choose which line of input to enter into the output. Any combinational circuit can be implemented with a multiplexer. As seen in Figure 1, a MUX circuit has four inputs, two selection inputs, and has one output. There are numerous choose lines that limit the choice of any information line. The decision line determines the input line that is routed toward the output line. Relays or transistors might be used to create an analog circuit known as a MUX, which switches from voltage and current input to a single output, or it could be a logic-gate-based digital circuit that alternates between binary data [4].

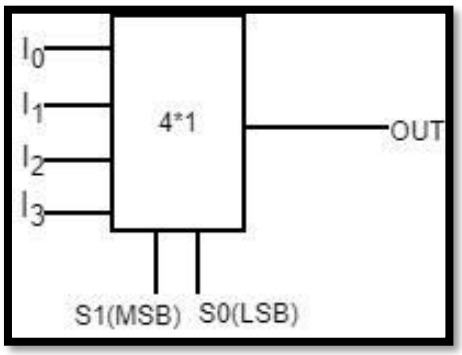

Fig.1.Basic block diagram for 4:1 multiplexer

2. System Design

2.1. GDI Based Multiplexer

In order to overcome shortcomings of the CMOS technology here in this research GDI technique used for the implementation for the low power combinational [6]. It has six transistors. Both the circuit for the CMOS inverter and the GDI (Gate Diffusion Input) circuit are similar, with the exception that NMOS is not attached to the ground and PMOS is not attached to the supply in the GDI, both of which are linked to inputs as seen in Figure 2. The GDI methodology is an additional low-power and area-efficient method in addition to conventional CMOS design [7]. The Figure 2 shows the schematic diagram of a 2x1 multiplexer. In this design, input A is an attachment to the PMOS source terminal, and input B is linked to the NMOS source terminal. The gate terminal (both MOS connected) works as a selection line.

For designing a 4x1 multiplexer, we can use two 2x1 MUX connected in parallel and one 2x1 MUX connected in cascade. The output of two 2x1 muxes is provided to cascade a 2x1 MUX as an output, As shown in Figure 3.

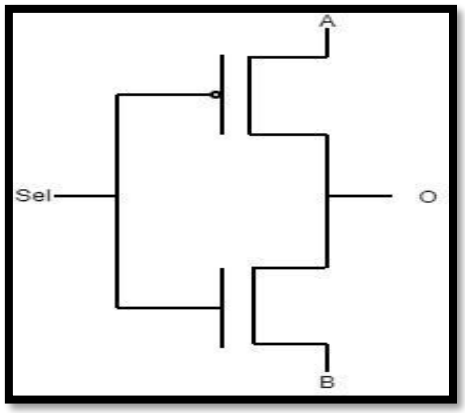

Fig. 2 GDI based multiplexer circuit

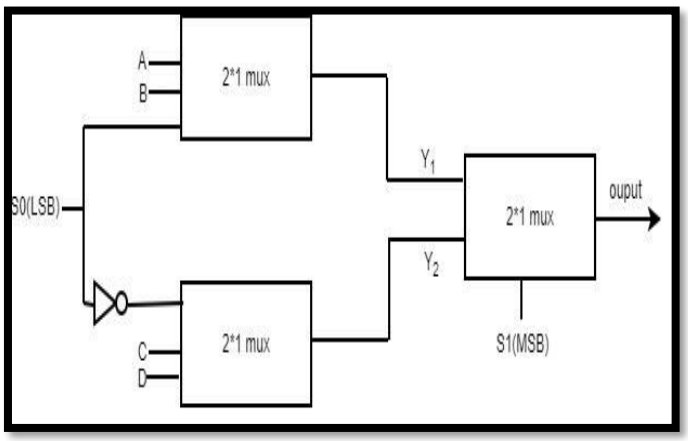

Fig. 3 Block diagram of 4:1 MUX using 2:1 MUX

2.2. Conventional CMOS-based multiplexer

Figure 4 depicts a conventional CMOS circuit, which is utilized in a variety of integrated circuit logic gates. These are made utilizing PMOS and NMOS Pull-Down Networks (PDN). Because of their straightforward design, they utilize minimal power, quick operating speeds, acceptable noise margins, and insensitivity to changes [8] [1]. However, there are times when different circuit families are required due to performance or space limits, and dynamic circuits are the most significant substitute.

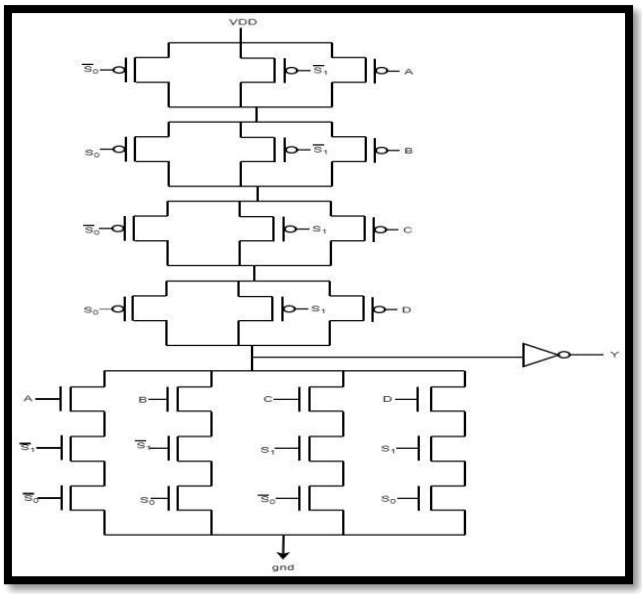

Fig.4 Conventional CMOS Based Multiplexer

As illustrated in Figure 4, a PUN (Pull-Up Networks) and a PDN are used to produce conventional CMOS logic. The PDN's job is to establish an output-to-VDD link; the timing of the logic gate's desired output is 1. Likewise, when the output is anticipated to be zero, the PDN links it to ground. In order for either PDN or PUN to operate in a steady state, the networks PDN and PUN are built in a way that exclude one another [9] [2]. Conventional CMOS logic has negligible quiescent power dissipation, which is one of its main advantages. For each applied input state, which might be the PDN or PUN, it stays inactive. This type of implementation takes more space to implement logic design, which affects capacitance and, consequently, the speed of the gate [1].

The PDN in pseudo NMOS logic is similar to that of a standard gate; however as shown in the Figure 4 (b), the PUN has been swapped out with a single PMOS transistor that is grounded to keep it always ON. In order to balance the noise margin and the speed, the widths of the PMOS transistors are selected to be around one-fourth of the NMOS PDN's strength, or half of its effective width; the ideal size depends on the process. This decreases the quantity of area required for implementation logics, which raises speed. However, these pseudo-NMOS logics have a number of additional issues, including static power consumption, delayed rising transitions, and contention on the falling transitions.

3. Result Analysis

The GDI-based multiplexer's performance displays reduction in power dissipation, latency, and transistor count. Table 1, compares traditional CMOS-based multiplexer outcomes, makes it evident that the proposed GDI-based 4:1 multiplexer performs better than the conventional CMOS designs. The GDI 4:1 MUX uses 607.4581µW of power to satisfy low-power goals. Offers significant energy and space reduction at a speed that is on par with or faster than a traditional CMOS. It is ideal for 90 nm low-power selection fabrics; it provides notable energy and space reductions at a speed comparable to or faster than a standard

CMOS. When compared to the current CMOS conventional GDI designs, it is evident that the proposed 4:1 multiplexer based on GDI performs better. With lower power consumption, lower latency, smaller size, and superior energy efficiency, the suggested GDI-based 4:1 multiplexer performs better than the traditional CMOS architecture. All things considered, it provides a small, low-power, high-performance solution that is perfect for contemporary VLSI applications, as shown in Table 1.

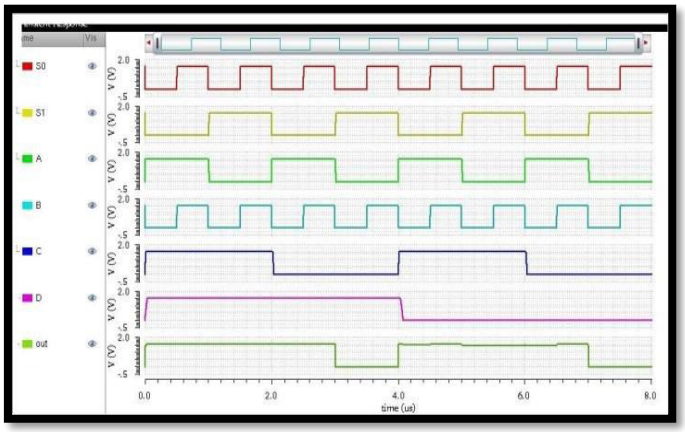

Fig. 5 Simulation Result of 4: 1 mux using GDI

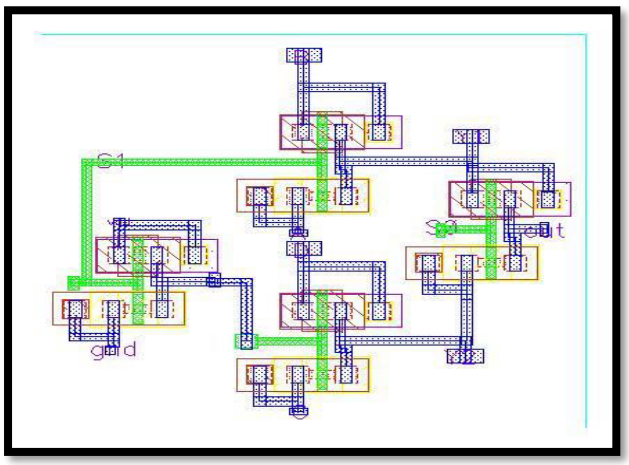

Fig.6 Layout of 4:1 mux using GDI

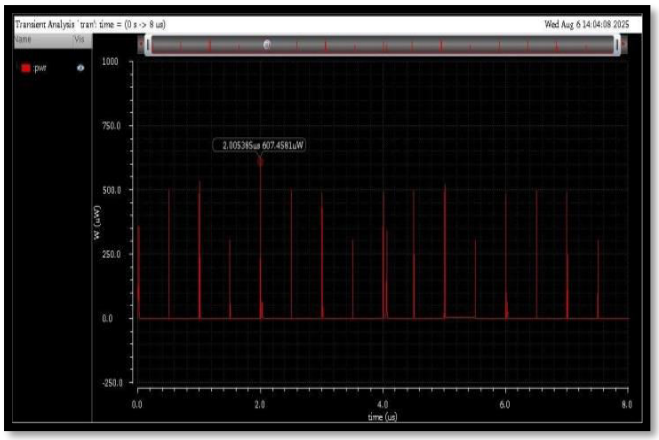

Fig. 7 Power Dissipation GDI

Tab.1: Comparison of 4:1 Multiplexer Designs.

Parameter	Conventional CMOS 4:1 MUX	Proposed GDI 4:1 MUX	Improvement
Technology Node	90 nm	90 nm	—
Power Consumption (μW)	1250.75	607.46	↓ 51.4%
Propagation Delay (ns)	12.4	9.6	↓ 22.6%
Transistor Count	32	16	↓ 50%
Power-Delay Product (PDP, Fj)	15.51	5.83	↓ 62.4%
Area (μm^2)	185	95	↓ 48.6%
Speed	Moderate	Comparable or Faster	—

4. Conclusion

The study successfully examined different 4×1 multiplexer designs implemented using 90 nm CMOS technology, focusing on power consumption, delay, and area utilization. The results clearly indicate that no single design outperforms others across all parameters; instead, each has its advantages depending on the design priorities. The MSL-based multiplexer demonstrates the least delay, making it suitable for high-speed applications. The conventional CMOS multiplexer has the lowest average power consumption, which is ideal for low-power designs. Meanwhile, the GDI based multiplexer offers the benefit of significantly reduced conventional power dissipation and area efficiency due to its minimal transistor count. Therefore, the optimal multiplexer design must be selected based on the targeted application requirements—whether prioritizing speed, power efficiency, or compact area. This comparative analysis emphasizes that technology-aware design choices are essential to achieving efficient digital systems in modern VLSI design.

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Author Contributions

A.B. developed the theoretical framework, designed the GDI-based 4×1 multiplexer architecture, and carried out the circuit simulations using 90 nm technologies. A.B. also performed the performance analysis, including power, delay, and transistor-count evaluation. B.C. contributed to the interpretation of simulation results, assisted in refining the comparative study between CMOS, GDI, and pass-transistor methodologies, and supported the manuscript organization. Both A.B. and B.C. contributed to writing, reviewing, and preparing the final version of the manuscript. B.C. supervised the overall project, provided technical guidance, and ensured the scientific accuracy of the research.

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