Design and implementation of an ultra-compact high performance prefiltered cascode5 ghz LNA in 90nm CMOS using a novel double split on chip IPD inductor for 5G Communications

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Abstract:
Low Noise Amplifier (LNA) is a major performance decider for any wireless receiver RF front end electronics (RFFE). Optimized system on chip (SOC) 5G LNA designs, primarily focus on minimal chip area via happy integration of low cost CMOS process and high quality IPD passives. **Approach:** This paper reports the fabrication of constant width and a novel double_ split multilayer (ML) IPD inductors designed to implement a compact 5 GHz LNA circuit in 90 nm CMOS for 5G applications. The LNA is designed with a three stage a cas code topology with an input 50 Ω matching pre filter, inductive source degeneration (ISD) stage followed by an output buffer. On chip CMOS inductors in an LNA were replaced with two proposed off chip IPD inductors. Three 5 GHz LNAs are simulated using Advanced Design System (ADS) software tool. **Findings:** The PCB inductor measurement results showed inductance and quality factor improvements of 232.14% and 55.78% over the CMOS inductor. The simulated 1.8 V LNA with double_ split inductor had exhibited outstanding performance by achieving: very good input matching $S_{11}$of -33.85 dB, very low S_{12} of -45.15 dB, high gain of 28.4 dB, very low Noise figure (NF) of 0.8 dB, higher IIP3 of 5.6 dBm, very low dissipation of 1.4 mW, excellent stability of 6.08 along with the least on chip area (OCA) of 0.08 mm^2. **Conclusion:** All these superior parameter enhancements clearly prove that the proposed LNA with 4 layer double_ split IPD inductor is highly suitable to realize a miniature high performance sub-6 GHz LNA for a 5G communication receiver.

Key Words: 1. LNA 2. CMOS 3. IPD 4. Multi Layer 5. Quality Factor 6. Prefilter 7. Cascode, 8. Common Source 9. Inductive Source Degeneration

Introduction

The extraordinary growth of high throughput 5G networks, user demands for smart wireless devices, the availability ofCMOS RFICs coupled with miniature integrated passive device (IPD) on chip passives, are the prime movers for focused research to realize system on chip (SOC) RF front end solutions. Globallydeployed ultra speed low latency 5G NR standardofferseMBB, mMTC and URLLCservices tosupport mission critical communication services like: LTE, IEEE 802.11 series WLAN, HIPERLAN II, UWB, GPS, WIFI, ZigBee, BT, massive IOT, M2M, D2D, remote healthcare, smart city projects, digitized logistics, mobile HDTV, augmented reality (AR), etc. The Sub-6 GHz spectrum (1 to 6 GHz) is popular5G industry choice, with NR N79 using 4.4 to 5 GHz and NR-U using 5.1 to 5.9 GHz spectrum.Advances in the Si based IPD passive technology successfully realized low cost onchip spiral inductor and capacitors to produce miniature 5G RFICs.But, these passives still occupy 70% of RFIC chip space. LNA design research tries to integrate theminiature IPD passives and low cost CMOS RFIC technology.

Being the first active gain component, the LNAis the directinfluencer of overall noise performanceof any receiver.It is still a big design challenge to simultaneously optimize thedesired parameters like minimum onchip area (OCA), small losses, input and output matching, smaller NF, and higher gain,high linearity, unconditional

stability.This work focuses to implement a 5GHzLNA by integrating theCMOS circuitwith miniaturized IPD passivesto achieve best LNA performance by careful iterative tradeoffs between all the process and geometry parameters of active parts and on chip passives.Specifically, active components of LNA circuit aredesigned and simulated on 90 nm CMOS technology, while the passive inductorsare realized in IPD process. This helped to reduce power loss smaller than CMOS process, but at very low chip space.
Past reported on chip passive's research proved the success of Si spiral inductorswith accurate inductance expressions for spiral geometries, optimized stacked spiral patterns to achieve high Q on chip inductors, multilayer on-chip spiral inductor that provides good LNA matching andvariable width on chip high Q inductor [1-4].Several successful research in the past had employed wide variety of LNA circuit designs selecting from: CMOS processes(TSMC/UMC - 60, 90, 130 and180 nm); amplifier configurations: Body floating and self bias, current-reuse, 2 to 3 stages, CS cascode and cascade structures;Transistors (NMOS,PMOS, FinFET, pHEMT), Matching networks (gyrator, bridged T coil, fractal,IPD and active inductors) [5-25]. These works have claimed performance enhancements to design parameters as: gain S21 in range (9.6 to 30.67); S11 (-8 to -33 dB); S12 (13 to -48 dB); Noise Figure (0.8 to 6 dB); Stability (1 to 5.1); 1 dB compression P1in (-4 to -18 dB); Linearity IIP3 (0.3 to -17 dBm); Power consumption (0.6 to 34 mW); Supply voltage (0.9 to 2.2 V); onchip area (0.34 to 52 mm^2) [5-25]. Each work reported significant improvements in few parameters but had poor performance in few other parameters, especially the occupied chip area and stability. This paper reports significant improvements achieved in majority of key design parameters while nearly close in others.

In order to achieve above goal, design aspects employed in this work are:inductively degenerated first stage CS cascode amplifier, gain boosting peaking inductor, Constant K passive 50 input matching prefilter, isolating second stage output buffer amplifier and optimal NMOS transistor channel length and width, etc.Here, we report a 4-6 GHz hybrid CMOS IPD LNA with least possible chip size, yet exhibiting excellent performance.

This paper is organized as follows. Technology, review of LNA techniques, LNA performance parameters and challenges in 5G LNA circuit designare explained in Section II. Section III discusses the proposed prefilter LNA, IPD passive design and fabrication, cascode ISD CS amplifier circuit design and output buffer operation. Section IV presents the simulation and measurement results of: fixed widthand 2_splitML IPD inductors for input matching network, CMOS LNA simulation, and the performance comparisons with previous research work results. In the final, Section V presents a conclusion of our research contribution.

LNA overall review:

In RFIC, LNA is a magic box with uncertain response beyond 1GHz.Very low power consumption is critical for mobile handsets. Several LNA designs developed employing different device technologies and circuit configurations from 1960-2020 have been reported in literature [5-25].

2.1 LNA Topologies and Techniques:

Prime LNA technologies employed the semiconductor processes like:microstrip, SAW, SiGe, Bipolar BJT, n-channel JFET, GaAs FET, MESFET, MMIC, CMOS, BiCMOS, MOSFET, MODFET, BiFET, FinFET, HBT, HEMT and pHEMTProcesses. CMOS and BiCMOS are popular below 10 GHz, while HEMT is employed beyond 10 GHz.Many previous LNA circuit designs employed are:1. Common Gate (CG) amplifier with local feedback (CGF) and a shunt feedback amplifier can enhance overall transconductance gm. 2. The current-reuse techniques use CS amplifier followed by Cascode stage toobtain high power gain, good stability and decrease power consumption. 3. Peaking inductor technique reduces the roll-off, enhance the bandwidth and achieve flatter gain. 4. Active inductor technique will make the LNA wideband. This is utilized to lower the output impedance, but may have low NF. 5. Filtering technique employs T match, Pie match, Constant K filter match for best possible impedance matching to enhance the gain and NF reduction. 6. Inductive source degeneration technique provides simultaneous input impedance matching and smaller noise. 7. Capacitive cross coupling technique with CS-CG cascade reduces miller effect for high gain and low NF.

2.2 Challenges in 5G LNA circuit design:

Multistandardfunction rich5G RF receiver designs must employ highly performing LNA in the RFIC.Presence of an LNA in receivers permit flexible tradeoffs so as toease the performance enhancements for the remaining building blocks of a 5G transceiver. Thus anLNA is a compulsory element in any modern 5G wireless receiver front end RFIC.Realizing a best performing onchip LNA is a big design challenge.

LNA design:

LNA increasesthe weakest antenna signal far above the noise floor, to yield best output SNR. To accomplish this objective, several design parameters for LNA circuit are defined and carefully optimized for best performance. Key LNA design parameters are: Process Technology, Center Frequency, Voltage/Power gain, Loss parameters (S11, S22), Noise Figure, Stability Factor, Linearity (1dB Compression point P1, 3rd order Intercept point IIP3), Supply Voltage, and on chip Area (OCA). The design specifications for proposed miniature C Band LNA are given in following table 1.

Table 1. Desired 5 GHz LAN specifications

LNA Parameter	Desired Specification
Technology	90 nm CMOS
Center Frequency f_0 (GHz)	5.0
Bandwidth (GHz)	4.8 to 5.2
Gain G (dB)	> 25.0
Noise Figure NF (dB)	< 1.5
Stability K	2 to 5
Input Return Loss S11(dB)	<-25
Reverse Isolation S12 (dB)	<-30
Output Return Loss S22 (dB)	<-10
1dB Input Compression Point P1 (dBm)	>-10
IIP3 (dBm) ~ (P1+10)	>0
P_{diss} (mW)	< 10
Supply Voltage (V)	1.5 to 2
On Chip Area OCA (mm^2)	< 0.1

The proposed LNA circuit is designed with three stages: 1. Input matching network, 2. Single stage cascode amplifier, 3. Output buffer stage, as shown in Figure 1. Second stage source degenerated cascode CS-CGamplifier topologybest ensures high forward gain, high linearity, low power consumption and low noise factor by minimizing the gain reducing evil miller effect of drain overlap capacitance (Cgd) [5].Gain of CS mode transistor M1 is stabilized with the negative feedback provided by itssource inductor (Ls). Gate inductor (Lg) of input CS transistor M1 helps in power match to preceding stage. Larger Lg reduces the noise factor also [13]. Both M1 and M2 transistors use same DC current through them and reduce current consumption. The cascode transistor M2 is provides good reverse isolation. The last stage CG buffer amplifier achieves good isolation, further gain and better LNA output impedance matching.

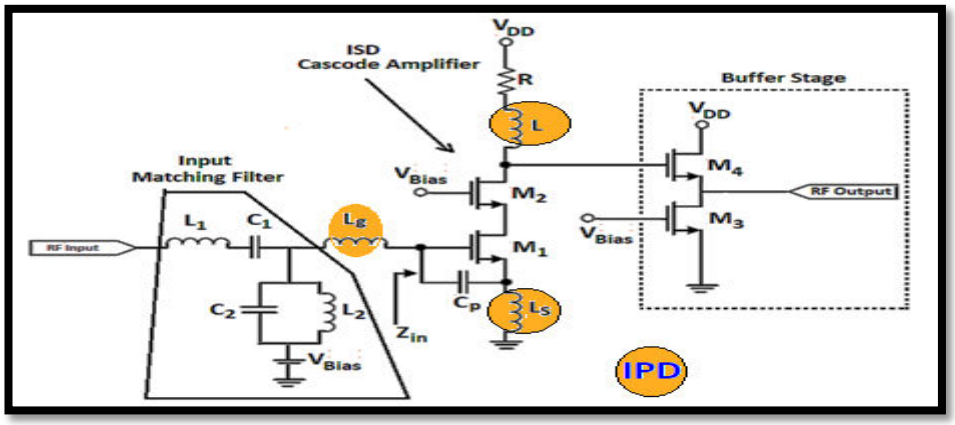


Figure 1. Single stage inductive source degenerated cascode LNA circuit with prefilter and output buffer

We need to choose the value of 'Cgs' of M1 for noise matching such that,

$$C_{gs} = \frac{2G_{opt}}{2\pi f} \quad (1)$$

Where G_{opt} is the optimum admittance of the source For alower NF, it is equal to 1/50 or 0.02. Thus Cgs shall be 1.2pF for this 5 GHz LNA.I nput matching network consists of C1, L1, L2,C2,Lg and Cgs1. Since the NMOS transistor has Cgs about 30fF, we choose to add a parallel capacitance Cp of1.2pF across the gate and the source. The resistance R is selected to ensure unconditional stable LNA up to 15 GHz. A carefully designed drain peaking inductor L of cascade transistor M2 resonates with overall drain capacitance so as to achieve maximum high frequency gain at tuned resonance.

The source and load impedances have been considered as 50 ohm. Degenerative inductor L_S sets the value of $Z_{in}$by tuning out gate-source capacitance C_{gs}. Lg tunes the input circuit at the desired resonance frequency .Inductance (Lg+Ls) and Cgs are resonated at 5 GHz center frequency to eliminate the imaginary part to achieve best input impedance Z_{in} match to 50Ω.Same IPD structure is selected for the high Q matching and biasing inductors L_S, L_g, and L, to minimize the loss plus overall chip size (cost) and also facilitate ease of fabrication. LNA is simulated with body-contacted NMOS transistors in 90 nm CMOS process, using ADS 2016.01 software that has NMOS transistor model parameters and the high Q passives. MOSFET has minimum gate length of 70 nm and a 0.3 V threshold voltage[25].

3.1 Design of input matching constant K bandpass filter:

The first stage is constant K band pass filter (BPF), which tunes the LNA to minimize input return loss (S11) for the best noise and power matching. Chebyshev Constant K filter is designed to simulate the 5GHz BPF, as shown in Figure 2, with the filter matched to the 50 Ωsource impedance (antenna).The inductors and capacitors used in LC resonators are L1 and C1 in series and L2 and C2 in shunt. Lg and Cgs1 are used to form a tank circuit at the source terminal of M1. All these tank circuits together form the50 Ωimpedance matching network.

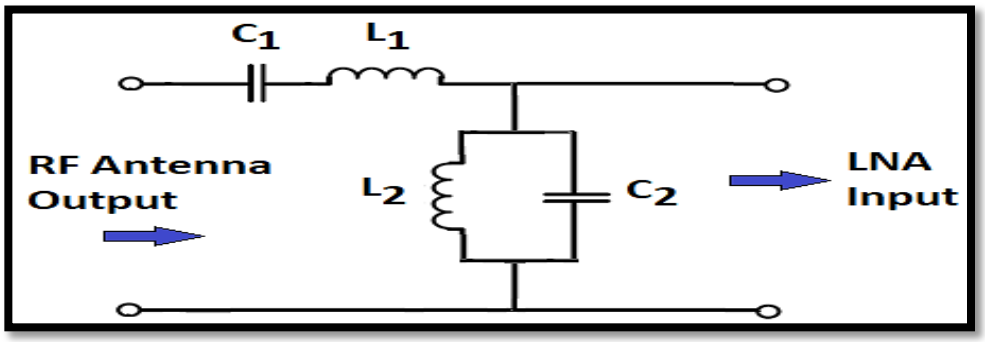


Figure 2. Input matching Constant K - LC Bandpass Filter

The inductor and the capacitor values are found by using f_0= 5GHz, f_2= 5.2 GHz; f_1= 4.2 GHz andZ_0= 50 Ω. Values of the series and shunt reactive components are computed from following equations.

$$L_1 = \frac{Z_0}{\pi(f_2 - f_1)} \quad (1)$$

$$L_2 = \frac{Z_0(f_2 - f_1)}{4\pi f_1 f_2} \quad (2)$$

$$C_1 = \frac{(f_2 - f_1)}{4\pi Z_0 f_1 f_2} \quad (3)$$

$$C_2 = \frac{1}{\pi Z_0(f_2 - f_1)} \quad (4)$$

The computed BPF component values are: L1= 26.5 nH, C1=38.3 nF, L2= 0.095 nH, and C2= 10.6 pF.

3.2 Design steps of the first stage cas code ISD amplifier components:

Inductive source degenerated cascode CS LNA configuration and its input equivalent circuit are given in Figure 3 (a) and (b). Input impedance is defined as ratio of input voltage (V_{in}) to input current (I_{in}) given in eq. (8).

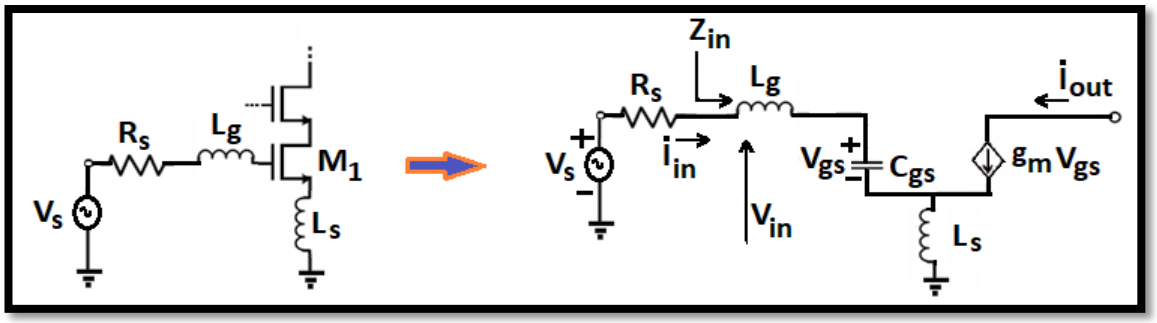


Figure 3. (a) The source degenerated LNA structure (b) its input equivalent circuit

$$V_{gs} = \frac{I_{in}}{sC_{gs}} \tag{5}$$

Assuming the parasitic resistances R_g, R_{Ls} and R_{Lg} as negligible, we have

$$V_{in} \cong I_{in}sL_g + I_{in}\frac{1}{sC_{gs}} + (I_{in} + g_m V_{gs})sL_s = I_{in}sL_g + I_{in}\frac{1}{sC_{gs}} + \left(I_{in} + g_m\frac{I_{in}}{sC_{gs}}\right)sL_s \tag{6}$$

$$V_{in} = I_{in}\left[s(L_g + L_s) + \frac{1}{sC_{gs}} + \frac{g_{mL_s}}{C_{gs}}\right] \tag{7}$$

Here, s is complex frequency, L_g is gate inductance, $L_s$is source inductance, $C_{gs}$is gate to source capacitance and $g_m$is transconductance of M_1.Now, the input impedance is

$$Z_{in} = \frac{V_{in}}{I_{in}} = \left[s(L_g + L_s) + \frac{1}{sC_{gs}} + \frac{g_{mL_s}}{C_{gs}}\right] \cong s(L_g + L_s) + \frac{1}{sC_{gs}} + \omega_T L_s \tag{8}$$

The condition to satisfy best50 Ω input impedance match, Re(Z_{in})must be equal to 50 Ω, while imaginary part Im(Z_{in}) is zero at f=f_0. Thus at resonance f=f_0, Ls and Lg are chosen to make the input match to Im(Z_{in}) =0, so that

$$j\omega_0(L_g + L_s) + \frac{1}{j\omega_0 C_{gs}} = 0 \implies \omega_0^2(L_g + L_s)C_{gs} = 1 \tag{9}$$

$$s(L_g + L_s) + \frac{1}{sC_{gs}} = 0 \implies \omega_0 = \frac{1}{\sqrt{(L_g + L_s)C_{gs}}} \tag{10}$$

For impedance matching, real part of Z_{in}must be equal to the source resistance R_s. It is expressed by:

$$Re[Z_{in}] = R_{in} = R_g + \frac{g_m}{C_{gs}} \cdot L_s = \omega_T L_s = R_s = 50\ \Omega \tag{11}$$

whereR_g is gate resistance of NMOS transistor, which is negligible. Source inductor $L_s$performs impedance matching. Gate inductor L_g sets input resonant frequency, as per equations (10) and (11).

$$Q_{in} = \frac{1}{wC_{gs}R_{in}} \tag{12}$$

Quality factor (Q_{in}) of input matching circuit at resonance is

$$Q_{in} = \frac{1}{\omega_0(R_s + \omega_T L_s)C_{gs}} = \frac{1}{2\omega_0 R_s C_{gs}} = \frac{\omega_0(L_g + L_s)}{2R_s} \tag{13}$$

Therefore capacitor voltage at resonance, is $V_{gs}=D_{in}.V_{in}$

Thus, the effective transconductance $g_{m1}$of this cascode LNA topology, is given

$$g_{m1} = \frac{I_D}{V_{in}} = Q_{in} * g_m = \frac{g_m}{wC_{gs}R_{in}} = \frac{\omega_T}{\omega_0\left(1+\frac{\omega_T L_S}{R_S}\right)R_S} \quad (14)$$

Where g_m is transconductance of M_1, R_{in} is 50 Ω input impedance and Q_{in} is quality factor of input matching network, ω_0 and ω_T are the center and transitionangular frequencies, respectively. Determine the unity gain angular frequency (ω_T) using eq.(11) by choosing appropriate value of L_s since R_s=50Ω. Now find the value of C_{gs} with eq. (11), using abov eω_T by taking g_m= 25 mA/V.Gate inductorL_g is found by substituting f_o, Cgs, and Ls in eq.(9).LNA input transconductance given by eq.(14). It is independent of actual transconductance g_m.

3.3 Computing the gain for LNA:

The gate-drain capacitance Cgd, and output resistances, R_{ds}, of transistors M1 and M2 are neglected to find the amplifier's voltage gain A_v. For a source inductively degenerated LNA in Fig.1, we put a lower bound on $g_{m1}$to ensure maximum gain.LNA voltage gain is determinedfrom Figure 3, as the ratio of Output and input voltages:

$$A_v = G_m * Z_l(\omega) = \frac{-G_m L_S}{1-\omega_0^2(L_g+L_s)C_{gs}+sG_m L_s} \quad \Longrightarrow G_m = \frac{I_{out}}{Vin} \quad (15)$$

$$A_v \cong Q_{in} g_{m1} Z_L = g_{m1} Z_{eq} = \left(\frac{1}{j\omega_0 L_s}\right)\left(\frac{j\omega_0 L}{1-\omega_0^2 L_1 C_0}\right) = \frac{L}{L_s}\left(\frac{1}{1-\omega_0^2 L_1 C_0}\right) \quad (16)$$

Relating eq. (10) and eq. (18), we find gain in simple form as

$$Gain\ in\ dB = 20\ log\frac{V_{out}}{Vin} = 20log\left(\frac{L}{L_s}\right) \quad (17)$$

Hence, drain inductor L must be chosen large enough to get maximum LNA gain. But, the value of L is technology dependent. Maximum inductance achievable for 90 nm CMOS process is 10 nH. Thus, to achieve proposed 35 dB gain, we shall determine L from eq. (17).

3.4 Noise Figure Evaluation:

Noise factor (F) is defined as ratio of input SNRto output SNR. Noise Figure (NF) is the noise factorF in dB.

$$NF\ dB = 10\ logF = 10\ log\frac{SNRin}{SNRout} \quad (18)$$

Noise figure for a source degenerated cascode common source LNA at 5 GHz frequency (f_o) is expressed as [13]

$$NF = 1 + \frac{\gamma}{g_m R_s}\omega_0^2\left(R_s C_{gs} + g_m L_s\right)^2 \quad (19)$$

Now substitute eqns. (10) and (15)in eq. (19) to obtain NF expression as

$$NF = 1 + \gamma\frac{4(g_m L_s)^2}{g_m R_s}\frac{1}{(L_g+L_s)C_{gs}} = 1 + \frac{4\gamma L_s}{(L_g+L_s)} \quad (20)$$

Here γ is the channel thermal noise coefficient and its value lies in range ($2 \leq \gamma \leq 3$). Thus the noise figure depends upon on L_g and L_s. Lower NF is obtained by selecting small L_s and large L_g.

3.5 Stability Analysis:

Any RF LNA is designed to be unconditionally stable. The Stern stability factor is used for NF analysis [23].

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2-|\Delta|^2}{2|S_{12}||S_{21}|} \quad \text{with} \quad \Delta = |S_{11}||S_{22}| - |S_{12}||S_{21}| \quad (21)$$

Here S_{11} (input reflection coefficient), S_{12} (reverse isolation), S_{21} (forward voltage gain) and S_{22} (output reflection coefficient) are the scatter parameters of any 2 port network. Any amplifier is stable if K>1 and $|\Delta|$<1. More recently K and Δ are equivalently replaced with parameter μ(μ>1 at the operating frequency) defined as

$$\mu = \frac{1-|S_{11}|^2}{|S_{22}-\Delta.conj[S_{11}]|+|S_{12}*S_{21}|} \quad (22)$$

3.6. Optimal width (W_{opt}) calculation for the LNA NMOS transistors:

The three important parameters of selected n-MOS transistor are V_{ds}, V_{gs} and I_{ds}. The desired value of I_{ds} is dependent on W/L ratio of NMOS transistor. Since we are using 90nm technology, minimum channel length (ℓ_{min}), is fixed at 90nm. First step is to calculate the optimum channel width (W_{opt}) of input transistor M1, which decides I_{ds} and NF. The maximum width of each transistor is called as optimal width (W_{opt}) to obtain best noise performance [13]. It is defined by

$$W_{opt} = W_{opt:F_{min}} = \frac{1}{3\omega_0 \ell_{min} C_{ox} R_s} \quad (23)$$

Here C_{ox} is gate oxide layer capacitance per unit area [F/m^2] defined as

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{K_{ox}\epsilon_o}{t_{ox}} \quad (24)$$

Where $\epsilon_{ox}$and K_{ox}=3.9 are the permittivity in [F/m] and relative permittivity of the gate oxide SiO_2. $\epsilon_o$is permittivity of the vacuum ($8.85*10^{-12}$)[F/m] and $t_{ox}$is gate oxide thicknesst_{ox} =$3.45*10^{-11}$ [m]. We find C_{ox} usingeqn. (24) and substitute it in eqn. (23) to find optimal width W_{opt}. The gate to source capacitance is

$$C_{gs} = \frac{2}{3} W_{opt} \ell_{min} C_{ox} \quad (25)$$

3.7. Analysis of power dissipation:

Biasing significantly influences the power consumption. Divergent voltage supplies (0.8 V, 1.1 V, 0.55 V and 1.8 V) are used to bias the circuit, so as to minimize the power consumption. Power wastage is minimized by using smaller bias voltage for input matching transistor M1. Gain boosting cascode transistor M2 is biased with higher voltage. Effective voltage V_{eff} applied to transistor M1 is the difference between V_{gs} (gate -source voltage)and V_{th} threshold voltage. Bias current is found from

$$I_D = \frac{1}{2} \cdot g_m \cdot V_{eff} = \frac{1}{2} \cdot g_m \cdot (V_{gs} - V_{th}) \quad (26)$$

Threshold voltage for an n-channel MOSFET is expressed as

$$V_{th} = 1 + \gamma\left(\sqrt{2\varphi_F + V_{SB}} - \sqrt{2\varphi_F}\right) \quad (27)$$

Here, V_{SB} is source - body voltage,V_{t0} is threshold voltage for V_{SB}=0. φ_F is process parameter lying in [0.3-2.4]. Power dissipation (P_D)is equal to $V_{DD}.I_D$. Transistor widths are carefully adjusted to reduce power dissipation. The LNA circuit consumes about 600 μA current from 1.8 V supply voltage at power dissipation around 1.4 mW.

3.8 LNA Component Selections:

The design of proposed LNA is done in TSMC 90 nm CMOS technology.Thus, all the NMOS transistors have same minimal length of 90 nm. Width W_1 of Transistor M_1 is selectedas 80 μm very close to the optimal width80 μm. The width $W_2$of cascode transistor M_2 is chosen as 70 μm(less than that of M_1)to minimize the parasitic capacitances. Cascode amplifier gain is controlled by the load inductor L and resistor R_L. Inductor and the width of transistor are optimized for minimum noise figure. The 50 Ω load driving buffer stage uses two transistors M_3 and M_4 (under saturation),with widths W_3 and W_4 found as 65μm and 50 μm. All these four widths are taken equal for cost effectiveness. Table 2 presents the list of optimized component values and

technology parameters for the designed compact high performance 5 GHz LNA circuit.To accomplish the chief objective of low cost, low power, low NF and least chip space the design constraints taken for the circuit components are listed below.

(1) $50 \leq W_1, W_2, W_3, W_4 \leq 100$ µm (2) $0.1 \leq Ls, Lg, L \leq 5$ nH(3) $20 \leq C_p \leq 30$ fF(4) $50 \leq W_{opt} \leq 100$ µm

Table 2. Optimized component values of proposed 5 GHz cascode CMOS LNA circuit

Component	Value
Input BPF – L1, L2, C1, C2	26.5 nH, 0.095 nH, 38.3 fF, 10.6 pF
Input Cascode – Ls, Lg, L	0.9 nH, 2.4 nH, 3.28 nH
Channel length ℓ_{min}	0.09 µm
Channel width W_{opt}	80 µm
W_1, W_2, W_3, W_4	80.16 µm, 70.25µm, 68.23µm, 57.95µm
V_{bias} (input transistor)	816.5 mV
V_{bias}(cascode transistor), V_{bias}(buffer stage)	1.1 V, 545 mV
Supply Voltage V_{DD}	2.2 V
Capacitances C_{ox}, C_{gs}, C_p	8.42 nF/m^2, 141 fF, 30.96 fF
Resistances R, R_s, R_L	60 Ω, 50 Ω, 50 Ω
Substrate-bias coefficient γ	2

Cascode LNA Implementation:

Proposed LNA circuit is simulated in 90 nm CMOS with ADS 2016.01software to operate at desired 5 GHz. LNA design and implementation is performed using both the on-chip and off-chip inductors and capacitors.

4.1 Input Matching BPF Simulation:

The reactive components L1, L2, C1, and C2of the Chebyshev Constant K band pass filter are calculated from the eqns. (1) to (4) using 4.8 GHz and 5.2 GHz (bandwidth of 400 MHz) as the upper and lower cutoff frequencies. The values of L_1=26.5 nH, L_2=0.095 nH, C_1=38.3 fF and C_2=10.6 pF are selected finally to obtain resonance at 5 GHz center frequency and also 50 Ω input match. The simulated ADS filter circuit is shown below in Fig. 4.

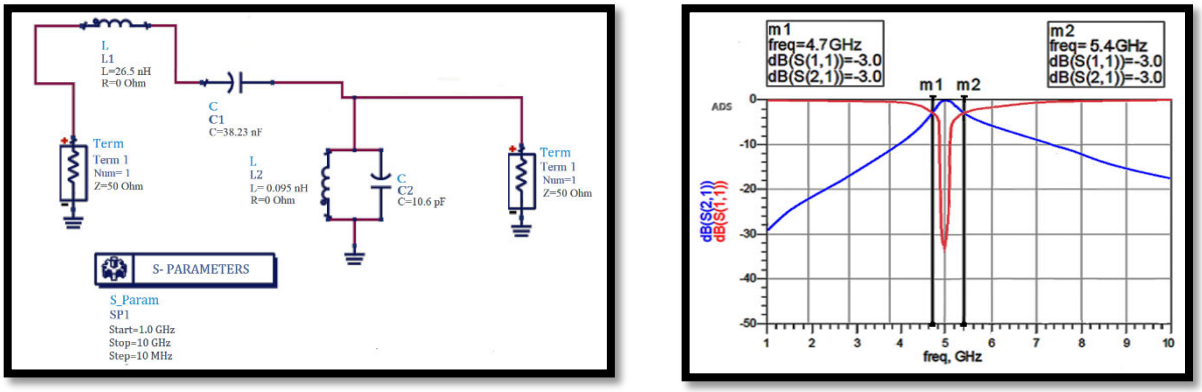


Fig. 4 (a) Simulated 5 GHz Chebyshev BPF in ADS **(b) Passband of BPF in C band**

The 3 dB Bandwidth of band pass filter is Δf=5.4-4.8= 0.6GHz as per Fig. 4(b), with a fractional BW of12%.

4.2 Simulation of Cascode amplifier inductors:

Both the onchip90 nm CMOSinductorsand offchip IPD inductors(Ls, Lg, and L)of first stage amplifier are designed and simulated in ADS (L_Model) and HFSSrespectively. Twotypes of onchip IPD MLspiral inductors(constant width and a novel double split inductor)for same chip area are designed, simulated and

fabricated.Their performance is tested to check for 5 GHz suitability.The ratio of outer to inner diameter is chosen in range [3,5] to enhance the quality factor and inductance at higher frequencies. Overall inductance of spiral geometry is given by modified Wheeler's formula.

$$L_{Total} = L_{Self} + \sum M_{+ve} + \sum M_{-ve} \quad (28)$$

The Q value of inductor is evaluated from Eq.(29) given as.

$$Q = \frac{\omega L_s}{R_s} \frac{1}{1+\frac{R_s}{Rp}\left(\frac{\omega L_s}{R_s}\right)^2 + 1} \left[1 - \frac{R_s^2(C_s+C_p)}{L_s} - \omega^2 L_s(C_s + C_p)\right] \quad (29)$$

ADS inductor model uses conducting copper material which has a relative permeability of 0.99991 and bulk conductivity of 5.8 x 10^7. IPD inductor model uses a 300 µm thick silicon substrate layer and 12 µm thin oxide layer to reduce losses and further the Q-factor. The Process and Geometrical parameters of our proposed inductors are given in table 3.Proposed inductors are designed in such a way that the mutual inductance is increased by splitting the conductor path width into two tracks by creating space between them. The geometrical and process parameters of the inductors are optimized to result in greater inductance and Q values.

Table3Process and Geometrical parameters of Spiral Inductors

Type of Inductor	Substrate	Number of turns	outer length (L1) µm	Conductor Width (W) µm	Conductor spacing (S) µm	Number of tracks per turn	On chip area mm^2
ADS CMOS (L_Model)	Copper	Microstrip Line					0.0324
IPD ML 3D Constant Width inductor	Si	4 (one full turn per eachlayer)	180	10	2	1	0.0324
IPD ML Double_split Inductor	Si	4(half turn per each layer)	180	4.5	2	2	0.0324

The L and Q values of these simulated inductors were found from the obtained S parameters via Y parameters employing following standard expressions.

$$Q = \frac{Im\,[Y_{11}]}{Re\,[Y_{11}]} \qquad L = \frac{-1}{2\pi f\{Im\,[Y_{11}\}]} \text{ and } \qquad R_s = \frac{1}{Real\,[Y_{12}]} \quad (32)$$

Here Y_{11}denotes short circuit input admittance, Y_{12} denotes short circuit reverse transfer admittance and Y_{22}denotes short circuit output admittance. Top view of geometrical structure for the two HFSS simulated inductors is shown in Fig. 6. The constant width and double splitting of each conductor turn into two separate tracks with in between spacing are reflected in this Figures 6 (a) and (b).

Fig.6.(a) Structure of ML Constant width Inductor b)Structure of Ml double Split Inductor

Optimized planar L inductances are obtained as Ls=0.9 nH, Lg=2.4 nH, and L=3.28 nH.Theplots for Inductance and quality factor oftwo IPD spiral inductors are given in Figure 7. The novelty of our proposed split inductor structure is its higher inductance and higher Q compared to the other inductors. Simulation results exhibited that the double split inductor showed1.73 timesincrease in inductance and 1.68 times increase in Q vale, comparedto that of the constant width inductor.

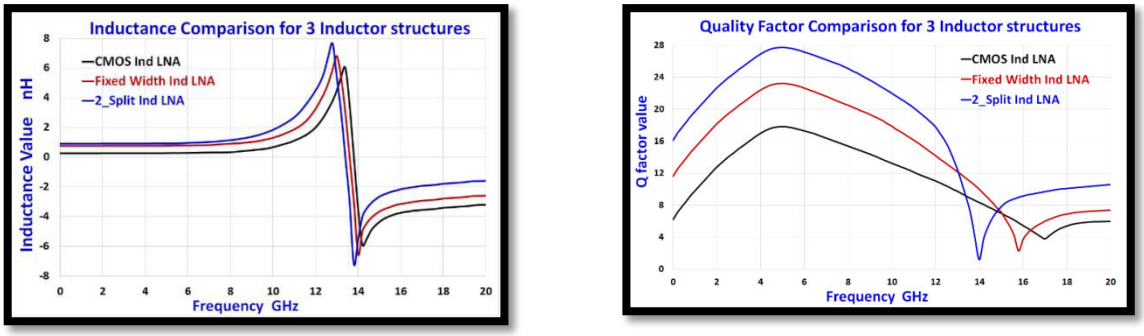


Figure 7.Inductance and Q value performance comparison for CMOS Spiral Inductor (L_s) ,IPD MLFixed width inductor $L_s$and IPD ML Double_split Inductor $L_s$in 3-6 GHz C Band

Table 4 summarizes the performance comparison of the proposed source inductors (L_s). It indicates that the double split inductor has very high inductance and Q factor compared with the reported inductors in past literature. Self resonant frequency (SRF) is found to be13.50 GHz, very much suitable for the present C band 5G implementations. Same trend was verified with the gate and drain inductors for (L_g and L) for the CS amplifier.

Table. 4 Performance comparison of CMOS inductor, IPD ML constant widthand IPD double_split ML Inductor in 3-6 GHz C Band

Type of Inductor	Center Frequency f_0 GHz	Inductance nH			Quality Factor Q			SRF f_R GHz	On chip area mm^2	Series Resistance Rs Ω		
		L_s	L_g	L	L_s	L_g	L			L_s	L_g	L
ADS CMOS Inductor (L_Model)	5.0	0.28	2.26	3.12	17.82	14.34	10.06	13.8	0.0324	50	50	50
IPD ML constant width inductor	5.0	0.78	2.39	3.18	23.25	20.46	15.85	13.6	0.0324	50	50	50
IPD ML Double Split Inductor	5.0	0.93	2.46	3.3	27.76	26.54	23.98	13.4	0.0324	50	50	50
Ref. 2	5.0	4.9			5.8			---	---	8.5		
Ref. 4	5.2	3.46			7.09			---	---	7.2		
Ref.5	5.0	10			15.12			---	---	5.0		
Ref. 13	5.0	3.23			9			---	---	100		
Ref. 22	5.0	0.4	3.7	2.2	7.8	22.7	20.2	---	---	---		

The proposed IPD inductors L_s, L_g and L are designed and simulated in HFSS. The CMOS onchip inductors designed in ADS are used in LNA simulation first and later replaced with IPD inductors for comparing performances.

4.3 Measurement results of two fabricated IPD inductors:

The IPD inductors are fabricated on four layer PCB with the FR4 substrate material. Its dielectric constant is 4.4 and area is16 ×16mm^2.The thickness of PCB is 1.60 mm with 0.15 mm copper thickness and metal layer spacing of 0.197 mm. The fabricatedConstant width and double split IPD inductorsare shown in Figure 8 and Figure 10.Corresponding test setup for experimental measurementsare shown in Figure 9 and Figure 11.

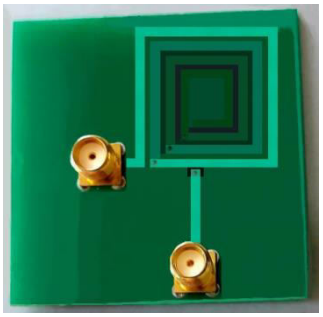


Figure 8. Constant Width Spiral Inductor Figure 9. Experimentation using a Network Analyzer

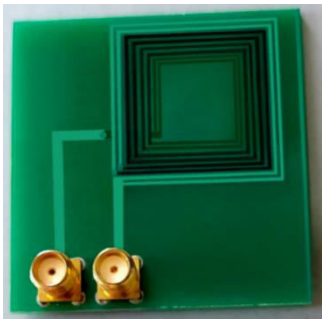


Figure 10. Double_ Split Spiral Inductor Figure 11. Experimentation using a Network Analyzer

Fabrication of compact µm scale inductors on silicon substrate is not available. The only available fabrication facility is amillimeter scale PCB. Hence technology scaling is done from micrometers dimension to millimeters, but retaining the similar geometry. So the inductor operating frequency is reduced from5 GHz to 150 MHz range. Proposed IPD inductors are simulated and fabricated in reduced mm scale to validate our model performance. The measurement results are obtainedusing Agilent Technologies N9923A vector network analyzer. Comparison of simulated and measuredvalues of inductances and Q factors for the proposed double split inductor structure are shown in Figure 12.

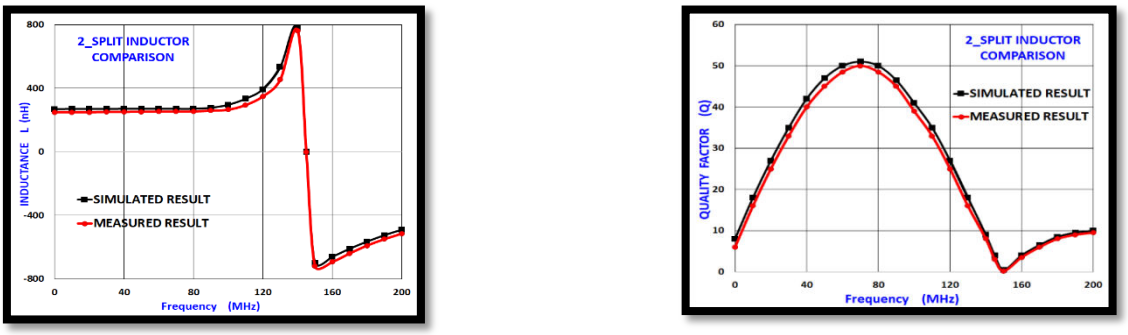


Figure 12. Simulation and measurement values of inductanceand Q factor of multilayer double split Inductor.

Table 5 presents the simulated and measured results for the constant width and double split inductors implemented on the multilayer PCB. It is well proven that PCB measurement results are in close matching with IPD simulation results. These results prove the supremacy of our novel split inductor structure to realize the easy to fabricate compact high performance onchip inductors for 5G applications even at micrometer scale CMOS process.

Table 5. Simulated results vs. measured results for the constant width and double split inductors

Parameter	ML constant width inductor		ML double split inductor	
	Simulation results	Measurement results	Simulation results	Measurement results
SRF f_0(MHz)	150	155	150	153
Inductance L (nH)	250	240	270	264
Quality Factor Q	45	41	50	48
Area (mm^2)	16x16	16x16	16x16	16x16
Width W (mm)	4	4	2	2
Spacing S (mm)	2	2	1	1

V Proposed 5 GHz LAN simulation using CMOS and IPD inductors:

The LNA is implemented at 5 GHz (C Band) using ADS software. The Constant K input matching BPF has 3 dB passband from 4.7 to 5.5 GHz. The circuit implemented in ADS shown in the figure 13. Output buffer stage enables good output matching. The LNA is designed for the following specifications given by Table 6.

Table 6. Design specifications of 5 GHz prefiltered cascode source degenerated LNA

LNA Parameter	CMOS Technology	Center Frequency f_0 GHz	Return Loss S11 (dB)	Isolation S12 (dB)	Gain G (dB)	Noise Figure F (dB)	Stability Factor (K)	Input 1dB Compression P_{1in} (dB)	IIP3 (dBm)	Power Consumption (mW)	V_{DD} Supply Voltage (V)	On Chip Area (mm^2) - Super Compact
Range	90 nm	5.0 (4.7-5.5)	< -20	< -20	> 25	< 2.0	2 to 5	-20	2-5	< 10	1.2 - 1.8	< 0.1

5.1 Implementation of LNA using onchip CMOS Inductors (Ls, Lg, L):

The LNA implemented in ADS using the designed components with onchip inductors (Ls, Lg, L) is shown in Figure 13. All the inductors are simulated using same CMOS model. The simulated inductances for Ls, Lg, and L are 0.28nH, 2.26 nH and 3.2 nHrespectively.Size of cascading transistor M2 is chosen similar to that of input transistor M1.

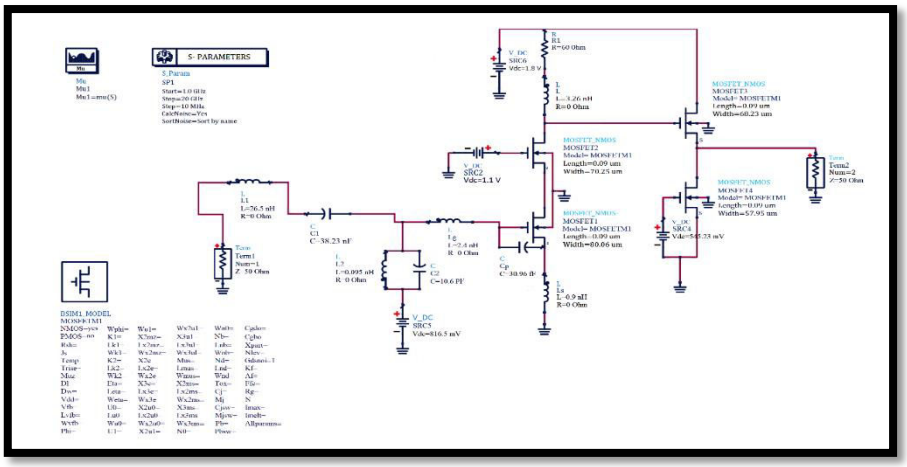


Figure13.
ADS layout of the source degeneration 5 GHz LNA circuit using CMOS inductors.

The inductors Ls, Lg, and L aresimulated in HFSS at layout level using IPD multilayer structures as shown in Figures 8 and 10.These inductorsin Fig.13, are replaced by four-layer constant width and double split structures,

respectively. The onchip area is180 µm × 180 µm.The ADS layouts of the source degeneration LNA circuit using above two IPD inductor structures are shown in Fig. 14 and Fig. 15.

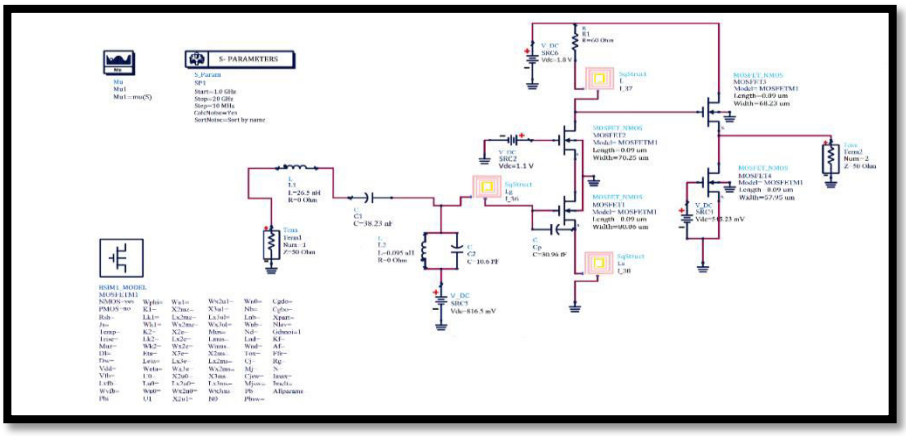


Figure 14. ADS layout of source degeneration 5 GHz LNA circuit using constant width IPD inductor

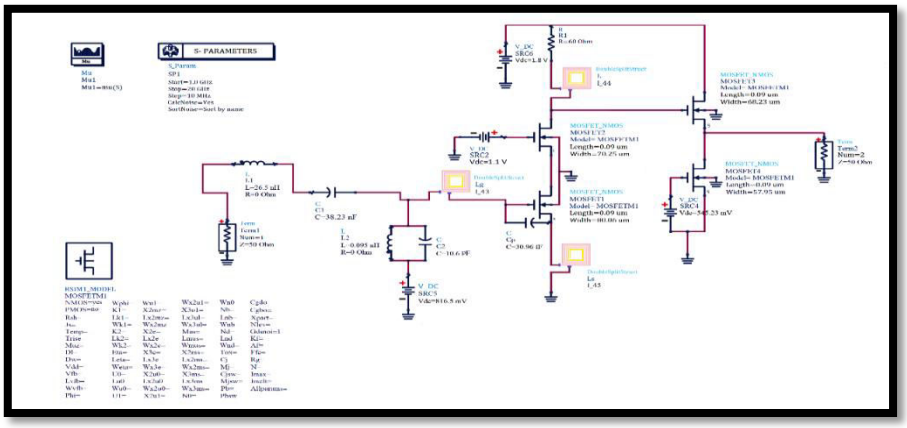
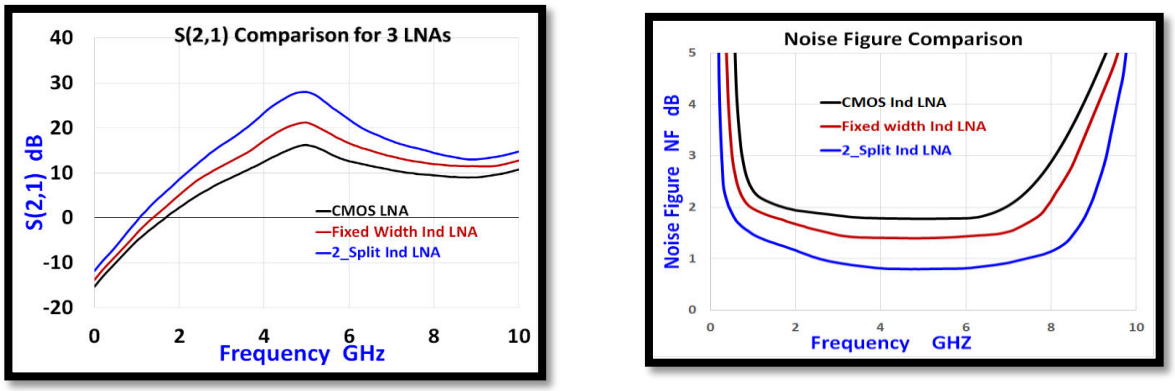


Figure 15. ADS layout of source degeneration 5 GHz LNA circuit using double split IPD inductor

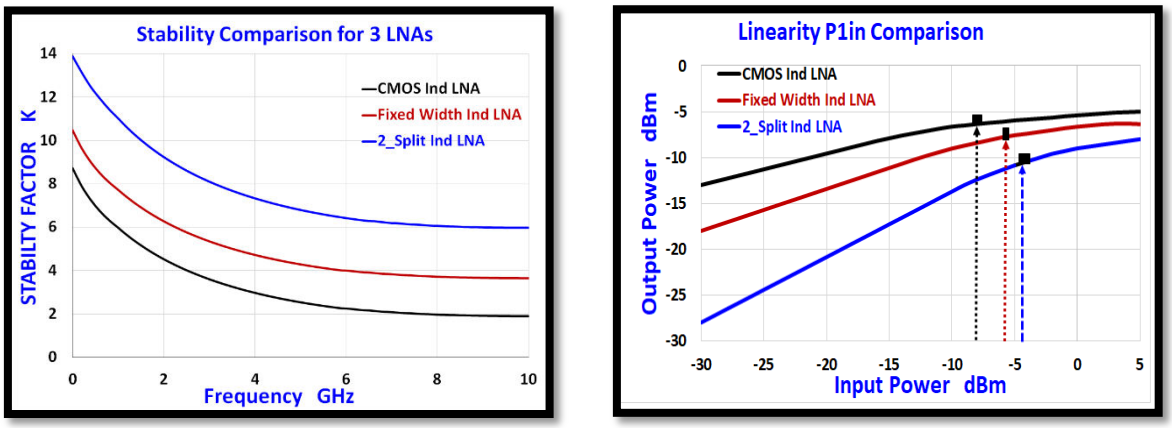
The inductance and quality factor performance of both type of IPD structures exhibited similar response trends, with the CMOS inductor simulated in ADS. Better performing double split IPD inductor results were shown in Figures 7 and 12, at both µm and mm technology scales. The orthogonal geometry of multiple vertical metal layers produced superior inductor performances by reducing the negative mutual inductance and the series resistance (Table 4). Thus, proposed 5GHz LNA using the IPD double split inductor structure exhibited excellent input matching with very small input return loss (S_{11}) of -33.85 dB as shown in Fig. 16. It also had very small 0.8 dB noise figure as shown in Fig. 17. This is due to gate inductance (L_g) being larger than source inductor (Ls). LNA peak gain from simulation result is 28 against the design value (>25), as given in Fig. 17. LNA is stable throughout the range from 4.5 to 5.8 GHz as K>1, reflected in figure 18. Also IIP3 is 5.6 dBm. Higher the IIP3 value, the better the linearity. This LNA has smaller power dissipation of 1.4 mW from 1.8 V supply voltage, as g_m is very small. Proposed LNA possessed the least occupied on chip area of 0.08 mm^2, when compared with recent reported LNA literature. Its fractional bandwidth is 16% (<20%) and hence a narrow band 5 GHz LNA [13].

(a)Figure 16. S Parameter comparison of three LNAs (a) Input Return loss S_{11} (b) Reverse isolation S_{12}



(a) (b)

Figure 17. Gain and Noise FigureComparison of three proposed LNAs (a) Gain S21 (b) NF



(a) (b)

Figure 18. Stability and P1in compression point comparison of three LNAs (a) Stability K(b) P1in

V. Conclusion:

The proposed novel double split IPD source inductor (Ls)showed excellent inductance and quality factor improvements of 232.14% and 55.78%respectively over that of CMOS inductor. Similar trends are visible for gate and drain inductors also (Table 4). The proposed novel multilayer constant width and double split IPD spiral inductor structures are designed, fabricated and tested successfully on a multi-layer PCB. The PCB measured results are in very good agreement with simulation results, demonstrating the superiority of our design. It is proved that the proposed 2_split inductor is highly suitable for making an on chip RFIC inductor in 90 nm CMOS process. The three inductors are used to design and simulate 3 LNAs for C band 5G front end in 4-6 GHz. Inductor and LNA simulations are carried out in HFSS and ADS software in 90 nm CMOS technology. Our designed three LNAs employing CMOS and IPD inductors demonstrated superior performance in the desired 4.7-5.5 GHz operating frequency range. Especially the LNA using novel double split IPD inductor designed for three inductors (Ls, Lg and L) had outstanding performance by achieving high gain of 28 dB, low NF of 0.8 dB, excellent input matching of -33.85 dB, very low S12 of -45.15 dB, excellent stability of 6.08, higher IIP3 of 5.6 dBm, lower power dissipation of 1.4 mW at 1.8 V supply voltage, and finally the least occupied chip space of only 0.08 mm^2. Table 7 presents the performance comparison of the proposed LNAs shown above with similar high performance LNAs from competing research works [6-12, 14-24]. All such superior parameter enhancements clearly prove that the proposed LNA with double split IPD inductor is highly suitable for the popular Sub- 6 GHz C band 5G wireless communication frequency standard.

Table 7. Summarized performance comparison for proposed LNAs with recent reported LNAs @ 5GHz

Our Work *Three 5.0 GHz LNAs*		**Techn-ology**	**f_0 (GHz)**	**S_{11} (dB)**	**S_{12} (dB)**	**S_{21} (dB)**	**NF (dB)**	**Stability Factor (K)**	**1 dB $P1_{in}$ (dB)**	**IIP3 (dBm)**	**P_D (mW)**	**V_{DD} Supply (V)**	**On Chip Area (mm^2)**	**Topology**
Design Specifications		**CMOS 90 nm**	**5.0 :4.7-5.5**	**< -20**	**< -20**	**>25**	**<2.0**	**2-5**	**-20**	**2-5**	**<10**	**1.2-1.8**	**<0.1**	**NB, Cascode**
Our 3 proposed LNAs (2023)	**CMOS Induct**	**CMOS 90 nm**	**5.0**	**- 20.65**	**- 38.10**	**16**	**1.4**	**2.65**	**-7**	**2.6**	**2.5**	**1.8**	**0.08**	**NB, Cascode**
	Fixed Width Induct	**CMOS 90 nm IPD**	**5.0**	**- 29.92**	**- 42.25**	**19**	**1.2**	**3.26**	**-5**	**4.6**	**1.9**	**1.8**	**0.08**	**NB, Cascode**
	2_Split Induct	**CMOS 90 nm IPD**	**5.0**	**- 33.85**	**- 45.15**	**28**	**0.8**	**6.08**	**-4**	**5.6**	**1.4**	**1.8**	**0.08**	**NB, Cascode**
Ref. [6] JFC 2022		CMOS 180 nm	3.7-11.9	-8.5	-	9.6	3.86	-	-	0.3 -1.3	-7.3	1.2	0.34	WB, current reuse
Ref [7] CHT 2021		CMOS 180 nm	5.1-5.9	-	-	13.1	2.6	-	-	-7.4	14.2	-	0.52	NB, Cascode
Ref [8] JFC 2021		CMOS 180 nm	2.4-9.1	-10.1	-	10.7	3.41	-	-	-6.2	3.3	-	-	NB, body floating
Ref [9] JX 2021		CMOS 180 nm	5.5	-15.4	-	-12.4	3.1	-	-8	-12	-	1.0	5.2	NB, bridged T
Ref [10] YK 2021		CMOS 65 nm	5.1-5.9	-10	-	18	2.4	-	-10	-14	7.2	-	0.56	WB, current reuse
Ref [11] XJ 2020		CMOS 130 nm	2.5-4.9	-14	-48	22.1	1.8	2.4	-	high	1.42	1.2	-	WB, current reuse
Ref [12] Li R 2020		CMOS 65 nm	26	-16	-	17	3.65	-	-	-8.75	16.4	-	0.481	WB, CS cascade

Ref [13] TS 2020	CMOS 90 nm	27-30	-10.44	-	30.7	0.72	2.1	-	-	5	2.2	-	NB, Cascode
Ref [14] JWL 2019	CMOS 140 nm	5.1	-8	-	9.6	1.4	-	-	-	5	-	38.4	NB cascade
Ref [15] HKC 2019	180 nm IPD	2-11	-	-	12	3.4	-	-	-	12	1.2	0.36	WB, IPD inductor
Ref [16]HH 2019	CMOS 180 nm	5.0	-17	-34	21.9	1.04	5	-4	9	0.944	0.9	-	NB, Cascode
Ref [17] ARA 2018	CMOS 180 nm	2-5	-7 – -25	-	7-13	6-7	-	-	-9.5	1.8	1.8	2.25	WB, sub-threshold
Ref [18] ZK 2018	SISL pHEMT	5.15-5.85	-16	-35	23	0.8	-	-	-	34	-	52	NB, micro strip
Ref [19] SM 2017	CMOS 180 nm	5.5	-27.46	-29.19	22.1	0.79	-	-	-6.5	-	1.8	-	NB, ISD
Ref [20] MS 2016	CMOS 130 nm	6.0	10	-	17	5.5	1	18	-7.7	15.2	-	2.2	WB, current reuse
[21] RK 2015	CMOS 180 nm	5.0	-12.2	13	-12	3.5	1.0	-	-	11	-	4	NB, ISD
[22] AM 2012	CMOS 180 nm	5.0	-33	28	-	1.9	-	-7	5	12	1.5	-	NB, cascode
[23] AP 2012	CMOS 180 nm	5.5	-16.1	22	-22	2.5	5.1	15.12	-3	16	-	10	NB, cascode
[24] HHH 2008	CMOS 180 nm	5.2	-12.7	14.1	14.1	3.37	-	-18	-17.1	1.68	0.6	-	NB, folded cascode
[25] DL 2005	CMOS 90 nm	5.5	-14	19	-19	2.9	-	-11.5	-2.7	9.7	1.2	0.94	WB, ESD

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