Scope
Volume 14 Number 03 September 2024

Impact of Interface Trap Charges on the Electrical and Analog/RF Performance of Dual Material Junctionless Tree FETs

Divya Beebireddy[1*], Kaleem Fatima[2], and L. Nirmala Devi[3]
[1,3]Department of Electronics and Communication Engineering, University College of Engineering, Osmania University, Hyderabad, India
[2]Department of Electronics and Communication Engineering, MuffakhamJah College of Engineering and Technology, Hyderabad, India

Abstract: This study thoroughly examines the electrical behavior and analog/RF performance of the dual material junctionless (DM-JL) Tree FET by incorporating interface traps at the Si/SiO_2 interface. These interface trap charges, which can arise from stress or radiation-induced damage, have the potential to influence the transistor's operating point and overall circuit reliability. To assess the impact of these traps, various parameters are analyzed using the proposed device with single-k (SiO_2) and dual-k (SiO_2+TiO_2) spacer materials. The study finds that, at zero trap charges, the DC and analog/RF parameters are superior in the dual-k spacer device compared to the single-k spacer device. When positive (negative) trap charges are introduced, significant changes are observed: the I_{on}/I_{off} ratio by 26% (37%), the subthreshold swing (SS) by 1.48% (0.59%), and the drain-induced barrier lowering (DIBL) by 1.62% (2.43%) decreases (increases), respectively as compared to the device with no trap charges. Further, the study measures analog/RF parameters such as gate capacitance, cutoff frequency, and gain bandwidth product, both with and without interface trap charges. Results indicate that the device with dual-k spacers performs better with negative trap charges. The interface trap charges affect the device's performance more severely in the subthre shold region compared to the triode and saturation regions.

Introduction:

The growing importance of portable electronic systems, coupled with the necessity to manage power consumption in densely integrated VLSI (Very Large-Scale Integration) chips, has spurred the swift and innovative development of short-channel multi-gate devices over recent decades. This trend is driven by the need for efficient, high-performance devices that can operate within the stringent power and space constraints of modern electronics.As transistors continue to scale down in size, moving into the short-channel regime, they encounter several significant effects that can degrade their performance [1]. To address the challenges posed by short-channel effects (SCEs), innovative material and device architectures are essential.One such architecture that has garnered significant research interest is the double-gate field-effect transistor (DG-

FET) [2]. While DG-FETs offer promising solutions to mitigate SCEs due to their superior gate control, they also present significant challenges, particularly in terms of increased complexity and power consumption. These issues become more critical as technology nodes shrink below 100 nm, highlighting the need for continued research and innovation in device architectures and materials to overcome these limitations [3, 4]. FinFETs have gained traction as a superior alternative to traditional DGEFTs, thanks to their improved scalability and reduced short-channel effects (SCEs). Despite their widespread use in bulk number at the 22-nm technology node, FinFETsencounter challenges with leakage and SCEs, which become more pronounced as devices shrink beyond sub-7-nm nodes [5]. Gate-All-Around (GAA) FETs have emerged as a promising replacement to address these issues, especially for technology nodes smaller than sub-5 nm. GAA FETs offer substantial improvements in the ON-OFF current ratio and exhibit excellent gate controllability by fully surrounding the channel. Nanowire (NW) and nanosheet (NS) FETs, two advanced technologies in the semiconductor industry, exemplify the advantages of GAA devices, particularly their extensive gate control capabilities [6].Despite their benefits, NW FETs encounter several drawbacks, such as increased parasitic effects, reduced driving currents, and complex manufacturing processes. In contrast, NS FETs offer superior electrostatic properties, reduced SCEs and parasitic capacitances, larger widths, and improved reliability of device [7]. By utilizing vertical layer stacking, nanosheet architectures accomplish up to a 30% greater effective width (W_{eff}) compared to FinFETs, significantly enhancing their overall performance [8].

To overcome the limitations imposed by single-fin vertical layer stacking of narrow current paths in standard cells, a variable and wider channel width has been introduced, permitting greater ON current and providing more adaptable device design for future scaling. However, this approach can lead to the self-heating effect (SHE), which adversely impacts device performance [9]. To overcome these issues, a new technological advancement called TreeFET has been implemented. TreeFET technology enhances effective channel width (W_{eff}) per footprint by connecting the narrow channels using a fin-shaped bridge. This advancement is significant for achieving high-efficiency devices that surpass the performance levels of NSFET and FinFET technologies [10 - 13].

Conventional FETs face issues like complex manufacturing, inconsistent properties, high doping concentrations, subthreshold currents, and scalability challenges. Spacers in FETs manage doping profiles, adjust channel width, provide insulation, and reduce SCEs. Low-k spacers reduce parasitic capacitance and circuit delays [14], while high-k spacers improve electrostatic integrity. These spacer technologies are crucial for optimizing FET performance and fabrication. Spacers in semiconductor devices improve gate and drain junction performance and enable band-to-band tunneling (BTBT). While they can introduce delays, they stabilize electric field coupling and enhance electron flow. As device scale decreases, increased fringing capacitance can

impact power dissipation and performance negatively [15, 16]. Recent studies have observed reduced leakage currents and SCEs in dual-k spacers, which incorporate both low- and high-k materials [17]. However, there remains a limited amount of comprehensive research on the performance of Junctionless (JL) TreeFETs with different spacer configurations.

Additionally, Interface traps are defects found at the boundary between materials, such as the gate oxide and the silicon substrate in MOSFETs. These traps can capture and release charge carriers, which can adversely affect the device's performance and reliability. Sunil Rathore et al [18], found that increasing the acceptor trap desnity improved the electrical behaviour of nano sheet FETs. Conversely, a higher density of donor traps at the Si–SiO_2 interface deteriorated the device's performance. BhaskarAwadhiya et al [19],foundthe performance of ultra-thin body and buried oxide (UTBB) fully depleted silicon-on-insulator (FDSOI) field-effect transistors (FETs) can be significantly compromised by defect charges caused by stress or radiation exposure.MaissaBelkhiria et al [20], used finite element methods to show that compared to other multi-gate transistors, Gate-All-Around (GAA) FETs exhibit enhanced resistance to short-channel effects (SCEs) even with lower levels of trap charges. The remaining part of this manuscript is structured as follows: Section 2 provides an overview of the simulation environment and the structure of the proposed device. Section 3 presents the findings and discussions. Finally, Section 4 offers the conclusions drawn from the study.

Device description and Simulation Setup:

Fig. 1(a) and 1(b) respectively present a 3-D structure and a 2-D cross-sectional view of the DM-JL Tree FET along the cutline X-X'. The dimensions of the examined transistor, as listed in Table 1, adhere to the current International Roadmap for Devices and Systems (IRDS) requirements [21]. The experimental data were meticulously calibrated and evaluated against simulated data to ensure precise device simulations [22], as depicted in Figure 1(c).

Table I: Device Parameters used in Simulation.

Parameter	Value
Gate length (L_g)	12 nm
NS Thickness (T_{NS})	5 nm
NS Width (W_{NS})	15 nm
IB Height (H_{IB})	6 nm
IB Width (W_{IB})	4 nm
Metal 1 Work function ϕ_{m1}	4.9
Metal 2 Work function ϕ_{m2}	4.6
Single-k Spacer	SiO_2
Dual-k Spacer	SiO_2 + TiO_2

Silicon serves as the channel material in both the inter-bridge (IB) and nanosheets (NS) structures, while a composite gate oxide is composed of a stacked SiO_2 and HfO_2layer.Various simulation models are employed to ensure accuracy, including Drift Diffusion model is utilized to effectively represent carrier transport within the device. The drift–diffusion model is utilized to effectively represent carrier transport within the device. To accurately account for mobility degradation due to the thin silicon film, a thin-layer Lombardi mobility model is applied, considering the nanometer-scale thickness of the channel. The SRH model incorporates deep-level defects toassess the degradation in drive current caused by trap-assisted recombination. The spacer length (Lext), which is the distance from the gate to the source or drain, is set at 7 nm. For dual-k spacers, combinations of outer low-k and inner high-k dielectric materials are used, with each spacer segment having anLext/2 length. This configuration is designed to optimize device performance by balancing the benefits of high-k and low-k materials in reducing fringing fields and improving overall electrical characteristics

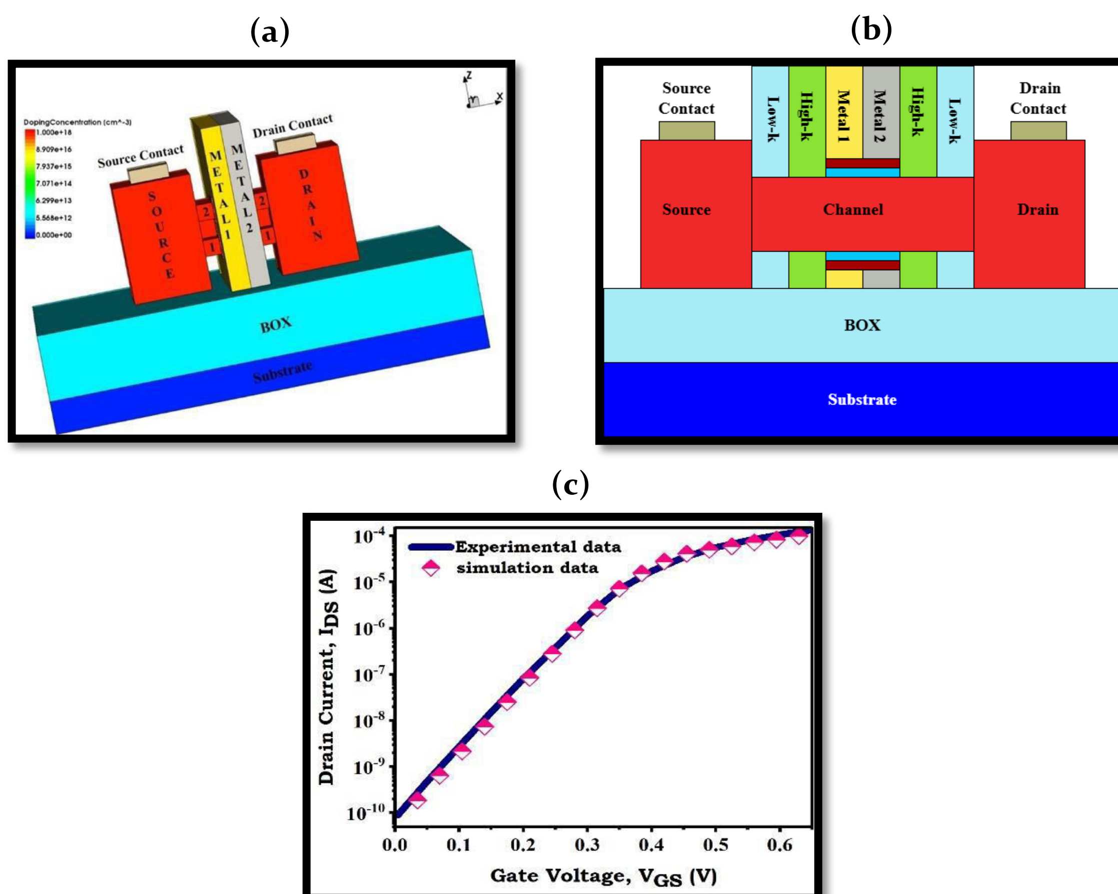

Fig 1. DM-JL Tree FET (a) 3D View (b) 2D channel view (c) Calibration with Experimental data [22]

Results and Discussions:

This study investigates how different interface trap charges (ITC) affect the various characteristics of the DM-JL TreeFET**. Figures 2 (a) and 2 (b)** illustrate the impact of ITC on the I_D-V_G characteristics for proposed device with both single and dual-k spacers.It was observed that with positive traps, both the I_{on} and I_{off} decrease, whereas negative traps cause an increase in these currents. This behavior is attributed to the shift in the device's threshold voltage caused by the trap charges. To mitigate fringing capacitance, a combination of single and dual-k spacers was used. Specifically, an SiO_2+TiO_2 spacer was employed to evaluate performance, revealing an improved switching ratio compared to the single-k spacer. This performance trend remained consistent with the presence of both positive and negative traps.

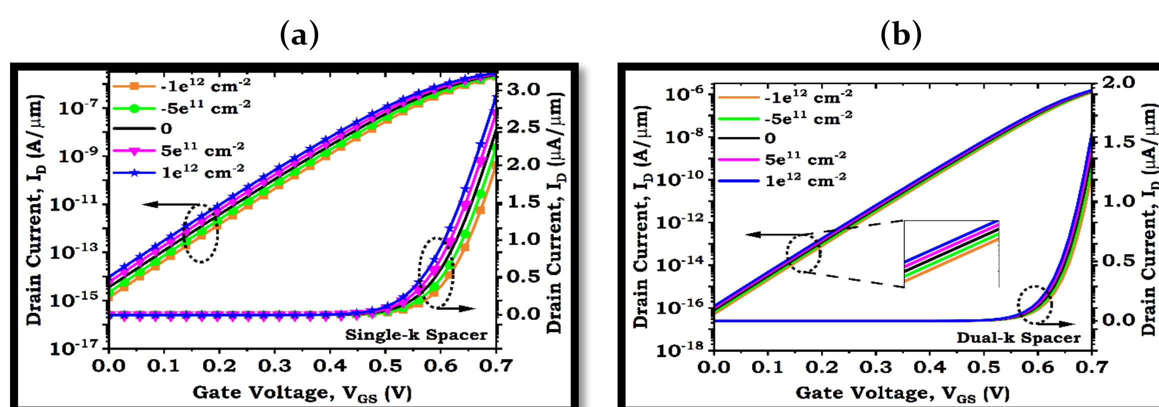

Fig 2. Impact of ITCs on Transfer characteristics of DM-JL Tree FET (a) Single-k Spacer (b) Dual-k Spacer

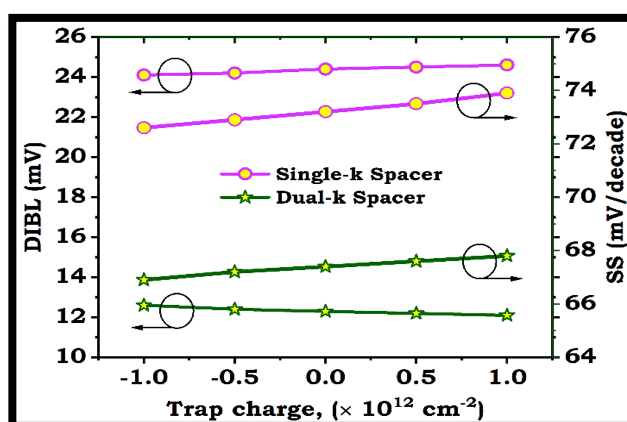

Fig 3. Impact of ITCs on SS and DIBL with Single-k and Dual-k Spacers

The subthreshold swing (SS) and drain-induced barrier lowering (DIBL) are two crucial metrics for assessing short-channel device performance. SS indicates how efficiently the device can switch on and off, essentially determining its switching speed [23]. On the other hand, DIBL measures the leakage current through the channel, providing insight into the device's leakage performance [24]. **Fig. 3** illustrates the variation of SS

and DIBL under the influence of ITCs with both single-k and dual-k spacers. The SS and DIBLvalues are noted to be low for dual-k spacers as compared to single-k spacers.The subthreshold swing, affected by ITCs, can be mathematically expressed as follows [25],

$$SS_{itc} = 2.3\frac{kT}{q}\left(1 + \frac{C_{dep}+C_{itc}}{C_{ox}}\right) \quad (1)$$

$$SS_{itc} = SS + 2.3\frac{kT}{q}\left(\frac{qN_{itc}}{C_{ox}}\right) \quad (2)$$

Where, C_{dep}, C_{ox} and $C_{itc} = qN_{itc}$ are the depletion, oxide and ITCs capacitances, respectively. From the equations it is observed that for the traps positive (negative) ITCs, the SS is increases (decreases) as shown in **Fig. 3.**

The presence of ITCs can greatly influence DIBL effect. ITCs, which are energy states at the interface between the semiconductor and the insulator, can capture and release charge carriers, altering the local electric field. Positive ITCs attract electrons, increasing local electron density and potentially enhancing the DIBL effect by lowering the threshold voltage and increasing leakage current. Conversely, negative ITCs repel electrons, which can mitigate the DIBL effect to some extent by raising the threshold voltage and reducing leakage as depicted in **Fig. 3.** However, negative ITCs might also negatively impact the device's on-state performance.

Fig. 4 illustrates the impact of ITCs on the transconductance (g_m) of the device with both single and dual k spacers. Transconductance is a critical parameter for the analog/RF performance of a device, as it measures the device's ability to control the output current with changes in the input voltage [26]. In the presence of positive ITCs, g_m increases for both dual-k and single-k spacers. This increase is attributed to the enhancement of the I_D-V_{GS} characteristics, as positive ITCs attract electrons, increasing the current flow through the device. Conversely, with negative ITCs, g_m decreases. Negative ITCs repel electrons, reducing the current flow and thus decreasing the g_m. This variation in g_m is directly related to the changes in the I_D-V_{GS} characteristics shown in **Fig.2**, where positive ITCs enhance and negative ITCs diminish the device's current flow.

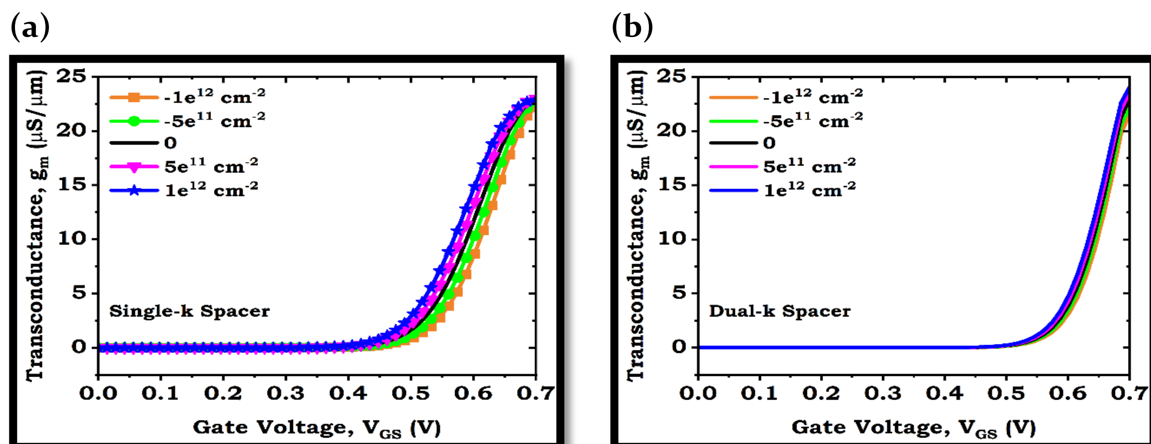

Fig 4. Impact of ITCs on g_m (a) Single-k Spacer (b) Dual-k Spacer

Additionally, we investigated the drain characteristics of the proposed device using both single-k and dual-k spacers. **Fig. 5** presents the effect of ITCs on drain conductance (g_d) of proposed device with both single-k and dual-k spacers, $g_d$which measures the variation of drain current with respect to the drain bias (V_{DS}). Achieving a minimal g_d is essential for enhancing the device's gain and overall analog performance. From Fig 5 the utilization of dual-k spacer in DM-JL TreeFET results in lower g_d in comparison with single-k spacer. Moreover, for positive (negative) ITCs result in a higher (lower) g_d compared to a device with no trap charges.

We have also examined the RF parameters of the DM-JL TreeFET under the influence of ITCs. Fig. 6 illustrates the variation in total gate capacitance (C_{gg}) with ITCs by considering both single-k and dual-k spacers. Our study found that devices with dual-k spacers exhibit lower capacitance compared to those with single-k spacers. This reduction in capacitance is attributed to the decreased fringing fields associated with dual-k spacers. When positive (negative) ITCs are present, they attract (repel) electrons towards the interface. This increase (decrease) in electron concentration near the gate oxide enhances the overall C_{gg}. The positive charges effectively add (diminish) to the gate's ability to store charge, leading to a higher (lower) capacitance.

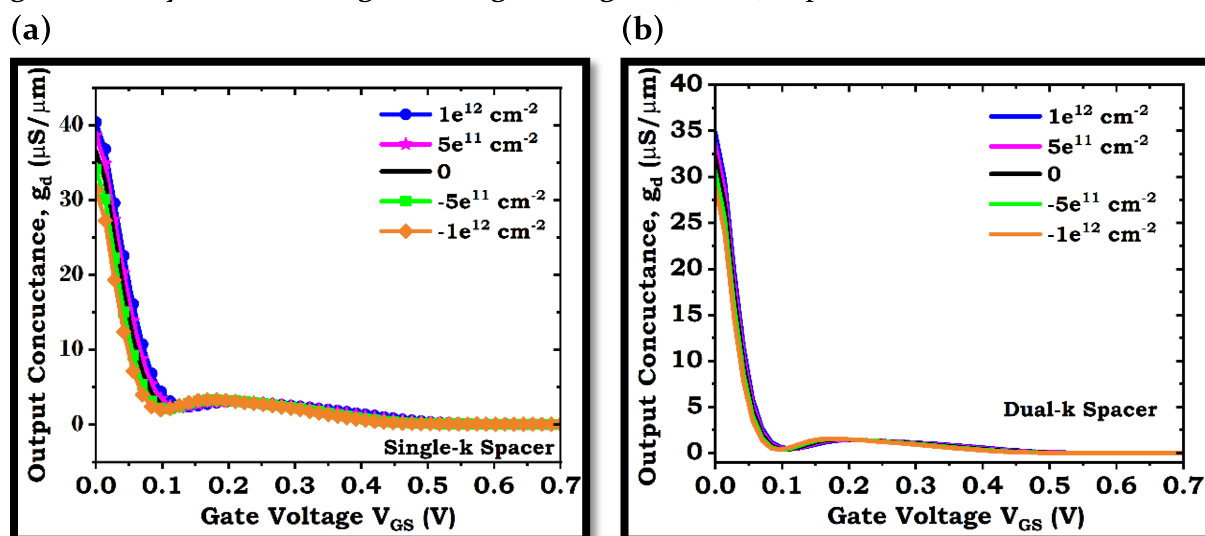

Fig 5. Impact of ITCs on g_d (a) Single-k Spacer (b) Dual-k Spacre

Fig. 7 depicts the intrinsic delay of the DM-JL TreeFET in the presence of ITCs with both single-k and dual-k spacers. Intrinsic delay is a critical parameter that dictates the speed at which the device operates. The study reveals that the intrinsic delay is more for with dual-k spacers as compared to single-k spacers and the intrinsic delay is minimized when positive traps are present and maximized when negative traps are present. This might be owed to the dominant increase (decrease) of the Cgg values with positive (negative) traps.

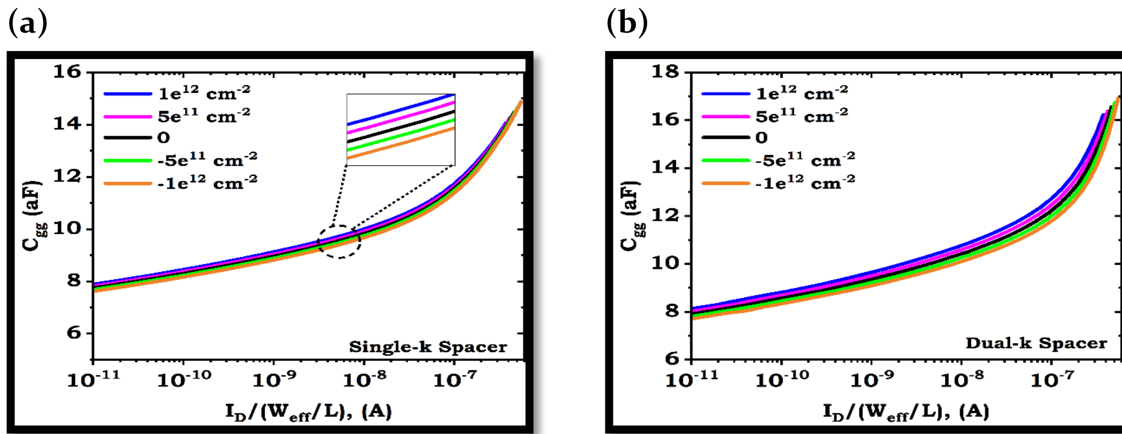

Fig 6. Impact of ITCs on C_{gg} (a) Single-k Spacer (b) Dual-k Spacer

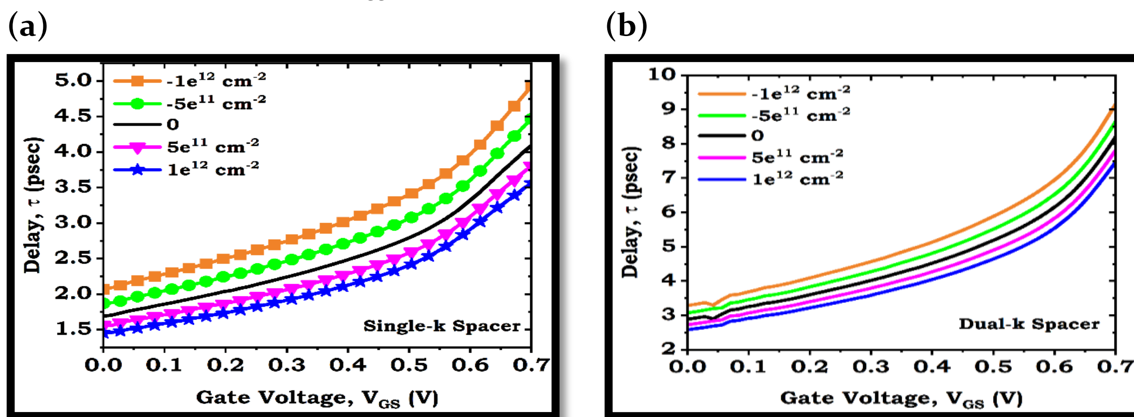

Fig 7. Impact of ITCs on Delay (a) Single-k Spacer (b) Dual-k Spacer

Fig. 8 demonstrates the influence of ITCs on the cutoff frequency (ft) of the DM-JL TreeFET with dual-k and single-k spacers. The ft is defined as the frequency at which the short circuit current gain of the device reaches unity. This parameter is crucial for determining the high-frequency performance of the device. When negative trap charges are present, the ft is lower compared to a device with no trap charges. This reduction in ft is due to the negative traps repelling charge carriers, which decreases the gm and increases the Cgg. Conversely, positive trap charges increase the cutoff frequency as they attract more charge carriers, thereby enhancing gm and reducing Cgg.

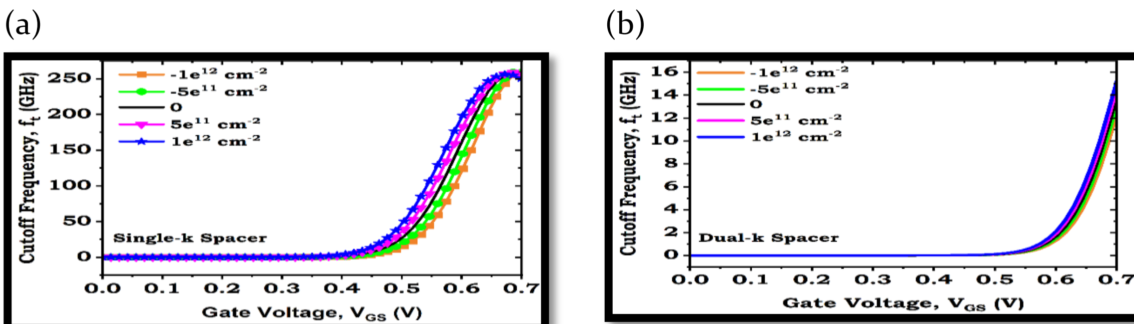

Fig 8. Impact of ITCs on f_t (a) Single-k Spacer (b) Dual-k Spacer

At lower gate bias, there is an initial enhancement in the f_t due to the increase in gm and the efficient charging of the C_{gg}. However, as the gate bias continues to increase, the f_t reaches a saturation point. This saturation occurs because both the g_m and C_{gg} reach their respective limits, preventing further improvements in cutofffrequency.Finally, **Fig. 9** illustrates the effect of ITCs on the gain bandwidth product (GBP) of the DM-JL TreeFET with both single and dual-k spacers. The GBP is a key performance metric defined as the product of the amplifier gain and its bandwidth. It provides an indication of the frequency range over which the device can amplify signals effectively.

$$GBP = \frac{g_m}{20\pi\, C_{gg}} \qquad (3)$$

The presence of negative (positive) trap charges results in a lower (higher) GBP compared to a device with no trap charges. This is because negative (positive) traps repel (attract) charge carriers, reducing (increasing) the g_m and increasing (decreasing) the C_{gg}, which negatively (positively) impacts the GBP. At lower gate biases, there is an initial increase in the GBP due to the improvement in g_m and efficient charging of the C_{gg}. However, as the gate bias continues to increase, the GBP reaches a saturation point. This saturation occurs because both the g_m and C_{gg} stabilize, limiting further enhancements in the GBP.

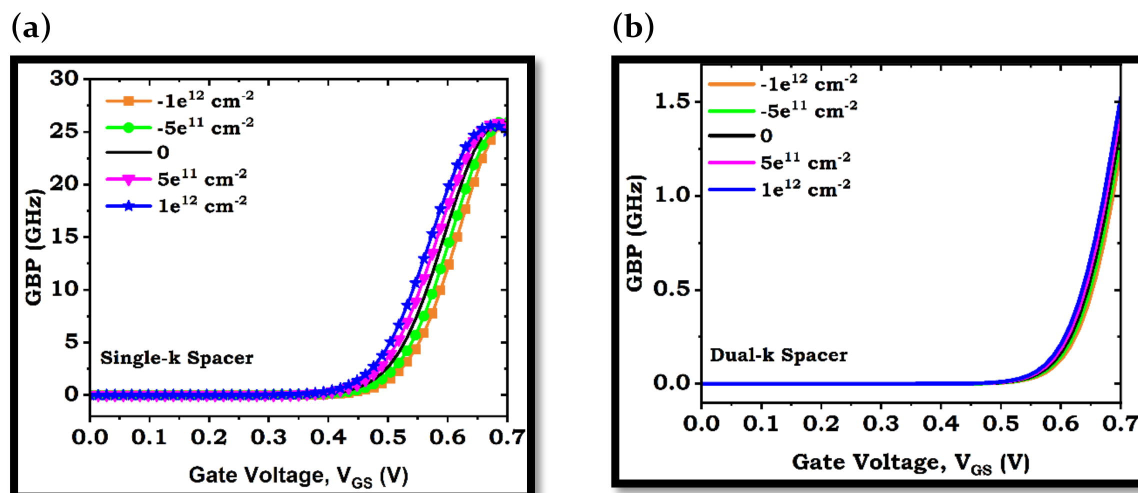

Fig 9. Impact of ITCs on GBP (a) Single-k Spacer (b) Dual-k Spacer

Conclusion:

In this the electrical behavior and analog/RF performance of the DM-JL Tree FET is investigated, emphasizing the significant impact of interface trap charges at the Si/SiO2 interface. Comparing devices with single-k (SiO_2) and dual-k (SiO_2+TiO_2) spacers, we found that the dual-k spacer outperforms the single-k spacer in DC and analog/RF parameters at zero trap charges. Positive trap charges degrade while negative trap charges enhance key metrics such as the I_{on}/I_{off} ratio, SS, and DIBL. Analog/RF

parameters, including gate capacitance, cutoff frequency, and gain bandwidth product, also show improved performance with dual-k spacers and negative trap charges. These findings highlight the importance of managing interface traps and selecting appropriate spacer materials to optimize DM-JL Tree FET performance, particularly advocating for dual-k spacers in mitigating adverse effects and enhancing device reliability.

References

1. H.S.P. Wong, Beyond the conventional transistor, Solid State Electron. 49 (5) (2005) 755–762.
2. S. Valasa, V.R. Kotha, N. Vadthiya, Beyond Moore's law – a critical review of advancements in negative capacitance field effect transistors: a revolution in nextgeneration electronics, Mater. Sci.Semicond. Process.173 (2024).
3. L. Chang, S. Tang, T. J. King, J. Bokor, and C. Hu, "Gate length scaling and threshold voltage control of double-gate MOSFETs," in IEDM Tech. Dig., 2000, pp. 719–722.
4. K. Boucart and A. M. Ionescu, "Length scaling of the double gate tunnel FET with a high-K gate dielectric," Solid-State Electron., vol. 51, nos. 11–12, pp. 1500–1507, Nov. 2007.
5. K. V. Ramakrishna, S. Valasa, S. Bhukya, and N. Vadthiya, "Optimizing U-shape FinFETs for sub-5 nm technology: Performance analysis and device-to-circuit evaluation in digital and analog/radio frequency applications," ECS J. Solid State Sci. Technol., vol. 12, no. 9, Sep. 2023, Art. no. 093007.
6. D. Nagy, G. Indalecio, A. J. GarcíA-Loureiro, M. A. Elmessary, K. Kalna, and N. Seoane, "FinFET versus gate-all-around nanowire FET: Performance, scaling, and variability," IEEE J. Electron Devices Soc., vol. 6, pp. 332–340, 2018.
7. J.-S. Yoon and R.-H.Baek, "Device design guideline of 5-nm-node FinFETs and nanosheet FETs for analog/RF applications," IEEE Access, vol. 8, pp. 189395–189403, 2020.
8. S. Valasa, S. Tayal, L. R. Thoutam, J. Ajayan, and S. Bhattacharya, "A critical review on performance, reliability, and fabrication challenges in nanosheet FET for future analog/digital IC applications," Micro Nanostruct., vol. 170, Oct. 2022, Art. no. 207374.
9. C.-J. Tsen, C.-C. Chung, and C. W. Liu, "Self-heating mitigation of TreeFETs by interbridges," IEEE Trans. Electron Devices, vol. 69, no. 8, pp. 4123–4128, Aug. 2022.
10. H.-Y. Ye and C. W. Liu, "On-current enhancement in TreeFET by combining vertically stacked nanosheets and interbridges," IEEE Electron Device Lett., vol. 41, no. 9, pp. 1292–1295, Sep. 2020.

11. C.-T. Tu et al., “Experimental demonstration of TreeFETs combining stacked nanosheets and low doping interbridges by epitaxy and wet etching,” IEEE Electron Device Lett., vol. 43, no. 5, pp. 682–685, May 2022.
12. Y. Sun, X. Li, Z. Liu, Y. Liu, X. Li, and Y. Shi, “Vertically stacked nanosheets tree-type reconfigurable transistor with improved ON-current,” IEEE Trans. Electron Devices, vol. 69, no. 1, pp. 370–374, Jan. 2022.
13. S. Valasa, S. Tayal, and L. R. Thoutam, “An intensive study of treeshaped JL-NSFET: Digital and analog/RF perspective,” IEEE Trans. Electron Devices, vol. 69, no. 12, pp. 6561–6568, Dec. 2022.
14. R. K. Baruah and R. P. Paily, “Impact of high-k spacer on device performance of a junctionless transistor,” J. Comput. Electron., vol. 12, no. 1, pp. 14–19, Mar. 2013.
15. V. B. Sreenivasulu and V. Narendar, “Performance improvement of spacer engineered n-type SOI FinFET at 3-nm gate length,” AEUInt. J. Electron. Commun., vol. 137, Jul. 2021, Art. no. 153803.
16. P. K. Pal, B. K. Kaushik, and S. Dasgupta, “Asymmetric dual-spacer trigateFinFET device-circuit codesign and its variability analysis,” IEEE Trans. Electron Devices, vol. 62, no. 4, pp. 1105–1112, Apr. 2015.
17. Y. S. Song, S. Kim, J. H. Kim, G. Kim, J.-H.Lee, and W. Y. Choi, “Enhancement of thermal characteristics and on-current in GAA MOSFET by utilizing Al2O3-based dual-k spacer structure,” IEEE Trans. Electron Devices, vol. 70, no. 1, pp. 343–348, Jan. 2023.
18. S. Rathore, R. Kumar Jaisawal, P.N. Kondekar, N. Bagga, Trap and self-heating effect based reliability analysis to reveal early aging effect in nanosheet FET, Solid State Electron. 200 (2023).
19. B. Awadhiya, S. Yadav, A. Acharya, Interface trap charges analysis on DC and high frequency characteristics of UTBB-FDSOI FET, Silicon 15 (2) (2023) 937–942.
20. M. Belkhiria, F. Aouaini, S.A. Aldaghfag, F. Echouchene, H. Belmabrouk, Investigation of trap density effect in gate-all-around field effect transistors using the finite element method, Electron 12 (17) (2023).
21. Hoefflinger B. ITRS: The international technology roadmap for semiconductors. InChips 2020: a guide to the future of nanoelectronics 2011 Oct 28 (pp. 161-174). Berlin, Heidelberg: Springer Berlin Heidelberg.
22. N. Loubet et al., “Stacked nanosheet gate-all-around transistor to enable scaling beyond FinFET,” Dig. Tech. Pap. - Symp. VLSI Technol., pp. T230–T231, 2017.
23. Babu KM, Goel E. Circuit Level Implementation of Negative Capacitance Source Pocket Double Gate Tunnel FET for Low Power Applications. ECS Journal of Solid State Science and Technology. 2024 May 22;13(5):053011.
24. Mudidhe PK, Nistala BR. Analytical modeling of a dual-material graded-channel cylindrical gate-all-around FET to minimize the short-channel effects. Journal of Computational Electronics. 2023 Feb;22(1):199-208.

25. Mudidhe PK, Nistala BR. Temperature analysis of DMGC CGAA FET for future deep space and military applications: an insight into Analog/RF/Self-Heating/Linearity. ECS Journal of Solid State Science and Technology. 2023 Aug 11;12(8):083005.
26. Mudidhe PK, Nistala BR. Impact of interface traps and noise analysis on dual material graded channel CGAA FET: A device reliability. Micro and Nanostructures. 2024 Jul 1;191:207850.