Design of F in FET based High gain Low Power Two Stage OTA for Biomedical Applications

Sarangam Kunamalla[1], and **Bheema Rao Nistala**[2]

[1] National Institute of Technology Warangal, Department of Electronics and Communication Engineering, Warangal, India

Abstract

FinFET transistors are the most suitable alternatives to conventional bulk transistors in sub 45 nm CMOS technology because of its improved behavior of short channel and sub threshold which are associated with low leakage current. In this paper, a two stage operational transconductance amplifier (OTA) is designed and implemented using FinFET devices employing composite cascode technique. In both input differential stage and output stage this technique has been used in biasing to make it operate in sub-threshold region to minimize the power dissipation and improve the gain of OTA. Moreover, frequency response and stability are achieved with indirect frequency compensation. The designed circuit is verified using cadence spectre in 18 nm FinFET technology. It requires 0.8V DC to provide an open loop gain of 100.43 dB, fT of 11.28 MHz with a 128 nW power consumption. The proposed circuit improved 36.25% gain, 82% UGB, 33% power efficient, and exhibits high figure of merit compared to conventional two stage OTA under same platform.

Keywords: FinFET, composite cascode, Low power, High gain, OTA, CMOS Analog to Digital Converter (ADC)

1. Introduction

In biomedical electronics, compact, portable, low-power equipment and wearable devices are desirable in recent years. A typical biomedical system consists of an instrumentation amplifier, analog filter and ADC. [1]. These operates on battery require low power dissipation for long battery life. The OTA is a critical analog building block used as a front-end instrumentation amplifier in biomedical systems. The characteristics required are minimum power usage, compact size, narrow bandwidth and high gain [2]. As a result, ongoing work and research in the field of low voltage low power OTAs is critical in order to keep up with developments in IC design. Scaling of transistor size limits the gain and bandwidth for minimal currents and low voltages also increased leakage current. As a result, designing efficient analog circuits with low bias voltages and compact channel devices will be challenging [3]. For increasing the gain various gain boosting techniques such as bulk biasing [4-5], floating gate transistors, level shifting and composite cascode transistors have been used in CMOS circuits [6-7]. In [8], body driven gain boosting is a new gain enhancement technique proposed. To achieve high voltage gain, a composite cascode connection was used for the input differential stage of operational amplifiers [9-10].

Though a two-pole system, a two stage OTA performs essentially as a single pole system, appropriate compensation techniques are used to place this pole beyond f_T. Simplest compensation is Miller compensation, which decouples the input and output capacitance. This capacitor eliminates the stability problem but creates a right half plane (RHP) zero. This RHP zero degrades the phase margin [11]. The techniques to eliminate right half plane zero are RC miller compensation, current buffer compensation [12], Split-output compensation [13] and cascode miller compensation [14]. A resistor and capacitor are connected in series in RC miller compensation. This RC compensation eliminates the right half plane zero but it requires ten times more current in second stage

than first stage i.e. it consumes more power and a large compensation capacitor is required. Current buffer compensation requires an additional stage which increases the power dissipation. Split-output compensation is an indirect way to compensate the Op-Amp but causes a stability problem due to linear region operation of transistor. Cascode miller compensation improves the stability with less power dissipation and small compensation capacitor.

In the present scenario of sub-50nm regime, the FinFETs find its edge in performance at par with planar MOSFETs. Beyond 45 nm technology conventional MOSFET suffers from short channel effects such as gate leakage current, velocity saturation, Drain Induced Barrier Lowering (DIBL), hot electrons [15]. Multi-gate transistors (FinFETs) have been used to resolve the issues [16-17]. Analog circuits using FinFET devices over that of CMOS devices is complex. FinFET provides good channel control, low current leakage, high output resistance, minimize effects of short channel, and high voltage gain and has CMOS compatible fabrication process. Some FinFET based two stage OTA architectures are reported in the literature. In [18], design and analysis of a two-stage OTA using SOI FinFET devices biased ina sub-threshold region for low power applications is presented. A novel architecture for high slewrate and fast settling OTA using 45 nm with 1 V supply voltage is proposed in [19]. In [20], a 22 nm LDD FinFET sigma delta ADC is designed. A 16nm FinFET high gain two stage operational amplifier is proposed in [21]. A bulk-drive technique for low voltage Independent Gate (IG) FinFET OTA has been designed in [22]. In [23], a two-stage self-biased OTA using IG FinFET transistors and gm/ID method is presented. These applications demonstrate FinFET transistors' utility in analog and mixed signal low voltage, low power circuits and systems.

This paper presents design and analysis of two stage OTA using FinFET transistors employing composite cascode technique for low high gain and also indirect compensation is used to increase the unity gain bandwidth and achieve the stability. FinFET devices, which are one of the most promising devices in modern Nano-scale circuits.

The remainder of the paper is structured as follows. The composite cascode structure and its small signal model used in the design of circuit are discussed in section 2. The proposed OTA circuit design and its analysis are described in section 3. In section 4, Simulation results are presented. Finally, conclusion is summarized in section 5.

2. COMPOSITE CASCODE STRUCTURE

Figure 1 depicts a single FinFET transistor that is equivalent to the composite cascode FinFET structure. They are made up of two series transistors, Mx and My, that share a common gate connection. This structure can improve the large effective output resistance and can also be used in low voltage analog circuits [2]. To prevent feed forward zero, a second accessible low impedance node (P) can serve as a miller feedback node or as a point for summing currents.

Based on the operating regions of Mx and My there exists three modes of operation. In case of first mode, the upper transistor (Mx) is biased in saturation region and lower transistor (My) is operating in triode region. This gives lower gain, high output impedance and higher bandwidth. In case of second mode, the upper transistor is biased in sub-threshold region and lower transistor is biased saturation region. This gives higher gain, high output impedance and low bandwidth. With low bias current, very high gain is achieved by biasing both transistors in the sub-threshold region. This region is useful for high gain and low power applications. For proper operation, the aspect ratio (W/L) of MX made higher than aspect ratio (mW/L) of MY, greater the multiplicity (m) of the aspect ratio larger will be the output resistance. The transfer and drain characteristics of composite cascode FinFET structure and equivalent single FinFET transistor for various values of m is depicted in Fig.2.For higher values of m, the composite structure behaves like a single transistor.

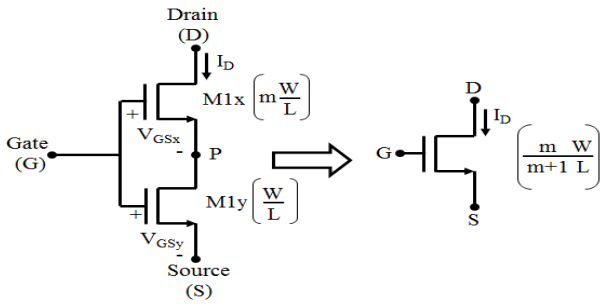
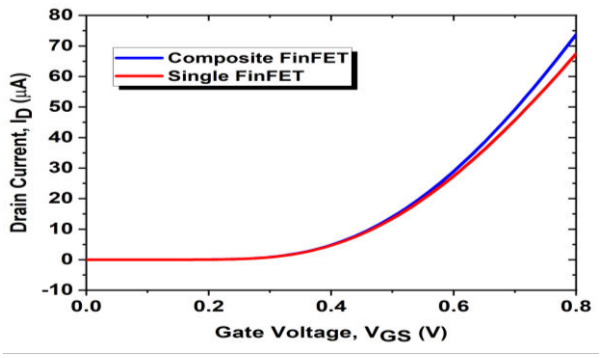
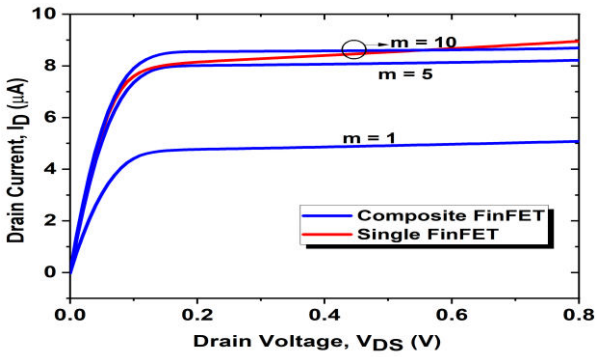


Fig. 1. Schematic of composite cascode structure



(a)



(b)

Fig. 2 (a). Transfer characteristics of composite cascode structure (b). Drain characteristics of composite cascode structure

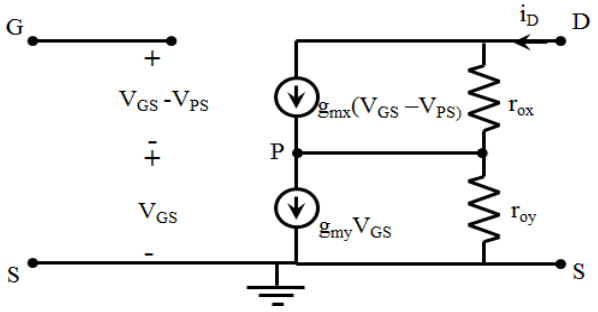


Fig. 3. Small model of composite cascode structure [10]

The small signal equivalent circuit of composite cascode FinFET structure is shown in Fig.3.Using this small signal model effective output resistance $R_{eff(out)}$ and effective transconductance g_{meff} is obtained. Assume that no body effect in the analysis i.e. VS and VB are tied to 0 Applying KCL at drain terminal (D), the small signal drain current (i_D) through the FinFET transistors can be expressed as

$$i_D = g_{mx}(v_{GS} - v_{PS}) + \frac{(v_{DS} - v_{PS})}{r_{ox}} \text{-------- (1)}$$

$$i_D = g_{my} v_{GS} + \frac{v_{PS}}{r_{oy}} \text{----- (2)}$$

Where g_{mx} and g_{mx} are the transconductance of M_x and M_y transistors respectively.$r_{ox}$and r_{oy} are the output resistances of M_x and M_y transistors respectively. The effective output resistance $R_{\text{eff(out)}}$ is defined by

$$R_{\text{eff(out)}} = \left.\frac{v_{DS}}{i_D}\right|_{V_{GS}=0} \text{ ---------- (3)}$$

From equations 1 and 2

$$R_{\text{eff(out)}} = (1 + g_{mx} r_{ox}) r_{oy} + r_{ox} + r_{oy} \text{---- (4)}$$

The product term $g_{mx} r_{ox} r_{oy}$ is dominating than other factors. Equation 3 is simplified as

$$R_{\text{eff(out)}} = g_{mx} r_{ox} r_{oy} \text{--- (5)}$$

The effective transconductance (g_{meff}) of composite cascode structure is defined as

$$g_{meff} = \left.\frac{i_D}{v_{GS}}\right|_{V_{DS}=0} \text{ ----- (6)}$$

From equations 1 and 2

$$g_{meff} = \frac{g_{mx} g_{my} + \frac{g_{mx}}{r_{oy}} + \frac{g_{my}}{r_{ox}}}{g_{mx} + \frac{1}{r_{oy}} + \frac{1}{r_{ox}}} \text{------ (7)}$$

The above equation is simplified as

$$g_{meff} = g_{my} \text{--------- (8)}$$

In composite cascode structure, lower transistor is dominating for effective transconductance (g_{meff}) and upper transistor is dominating for effective output resistance.

3. Circuit Implementation of Proposed OTA and its Operation

A. Two stage conventional OTA

The two stage OTA is the basic analog building block in biomedical system. Fig.4 shows the two-stage conventional OTA using FinFET transistors [11]. The first one is input M1-M5 differential stage and second one is common source M6-M7 output stage with a bias current of I_{bias}. Transistor (M8) is used to mirror the bias current. The second stage input to the output is connected with Miller compensation capacitance (CM). It has two poles and one zero. The following equations calculate the small signal DC gain of two stage OTA.

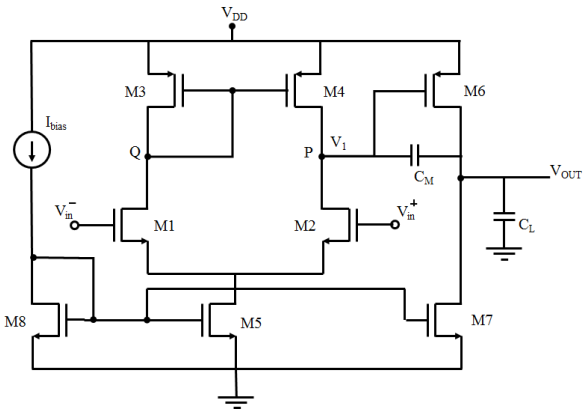


Fig. 4. Schematic of two stage conventional OTA using FinFET devices

The first stage dc gain is

$|A1|=g_{m2}\ R_1$----------(8)

Where $R_1= r_{ds2} \parallel r_{ds4}$

The second stage dc gain is

$|A2|=g_{m6}\ R_2$ ----------(9)

Where $R_2= r_{ds6} \parallel r_{ds7}$

Finally, the total dc gain is $A_o= A_1 A_2$

The circuit has two poles and zero, which can be obtained as follows. The first pole is

$P_1=\frac{-1}{g_{m6} R_1 R_2 C_M}$ ---------- (10)

The second pole is

$P_2=\frac{-g_{m6}}{C_L}$ ----------(11)

And zero is

$Z=\frac{g_{m6}}{C_M}$ ---------- (12)

The unity gain bandwidth and miller compensation capacitor is calculated by following equations

UGB=$\frac{g_{m2}}{C_M}$ ---------- (13)

$C_M \geq \frac{g_{m2}}{g_{m6}} C_L$

B. Proposed Composite Cascode Two stage OTA Structure

Fig.5 depicts the proposed two stage OTA using FinFET devices utilizing composite cascode structure in both the stages and indirect frequency compensation technique is used. The input stage and output stage are differential and single ended, respectively. In this circuit M1x, M1y, M2x, M2y, M3x, M3y, and M4x, M4y form a input differential stage and M6x, M6y, M7x, M7y form a common source amplifier output stage. Transistors M8x, M8y form a current mirror providing the bias current. The indirect frequency compensation is realized with Miller capacitance (CM) between the internal node (P) and the output. To minimize power dissipation all transistors should operate in sub-threshold region. Proper inversion coefficient (IC) of the composite transistors results in compact size, high gain and low power. Let us consider the transistors M1x and M1y, M2x and M2y, M3xand M3y, M4x and M4y, M6x and M6y, M7x and M7y forms composite cascode structures cc1, cc2, cc3, cc4, cc6 and cc7 respectively.

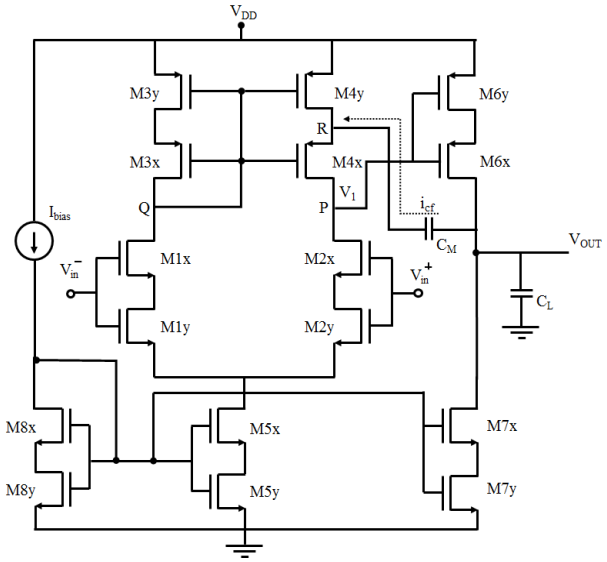


Fig. 5. Schematic of two stage proposed OTA using FinFET devices.

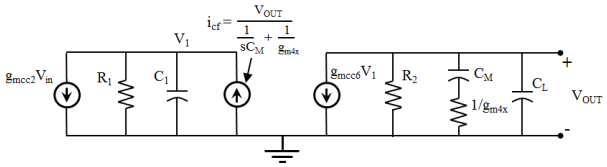


Fig. 6. Two stage proposed OTA's small signal model.

The transfer function of the two-stage proposed OTA is determined with the small signal model shown in Fig.6. Applying KCL at V_1 node and V_{OUT} node gives

$$-g_{mcc2}v_{in} + \frac{v_{in}}{R_1||\frac{1}{sC_1}} + \frac{v_{out}}{\frac{1}{sC_M}+\frac{1}{g_{m4x}}} = 0 \text{----- (14)}$$

$$v_{out} = -g_{mcc6}v_{in}X_2 \text{-------- (15)}$$

Where $X_2 = R_2||\frac{1}{sC_L}||\left(\frac{1}{sC_M}+\frac{1}{g_{m4x}}\right)$ is the total impedance at the V_{out} node. $\frac{1}{g_{m4x}}$ is the resistance looking at node, where the feedback current is injected. g_{mcc2} and g_{mcc6} are the transconductances of cascode structures cc2 and cc6 respectively. It is represented as

$$g_{mcc2} = g_{m2y}$$

$$g_{mcc6} = g_{m6y}$$

$$R_1 = R_{occ2}||R_{occ4}$$

$$R_1 = g_{m2x}r_{o2x}r_{o2y}\,||g_{m4x}r_{o4x}r_{o4y} \text{ ------- (16)}$$

$$R_2 = R_{occ6}||R_{occ7}$$

$$R_1 = g_{m6x}r_{o6x}r_{o6y}\,||g_{m7x}r_{o7x}r_{o7y} \text{ --------- (17)}$$

On solving equations 14 and 15, the proposed circuit transfer function is

$$TF = \frac{v_{out}(S)}{v_{in}(S)} = \frac{-A_v\left(1+\frac{S}{P_z}\right)}{\left(1+\frac{S}{P_1}\right)\left(1+\frac{S}{P_2}\right)\left(1+\frac{S}{P_3}\right)} \text{ ---------- (18)}$$

$$Where\ A_v = A_{v1}.A_{v2}$$

The first stage gain is $A_{v1} = g_{mcc2}R_1$

The second stage gain is $A_{v2} = g_{mcc6}R_2$

The overall gain of the proposed circuit is $A_v = g_{mcc2}g_{mcc6}R_1R_2$--------(19)

The first pole $P_1 = \frac{1}{g_{mcc6}R_1R_2C_M}$ ----------(20)

The second pole $P_2 = \frac{g_{mcc6}R_1C_M}{C_2\left(\frac{C_M}{g_{m4x}}+R_1C_1\right)}$-------(21)

$= \frac{g_{mcc6}C_M}{C_IC_1}$

The third pole $P_3 = \frac{g_{m4x}}{C_M}$ -------(22)

$z = \frac{g_{m4x}}{C_M}$ which is the left half plane zero

The f_T of the proposed circuit

$UGB = P_1A_v = \frac{g_{mcc2}}{C_M}$

4. Simulation Results

All the OTA circuits are simulated in cadence spectre in 18 nm FinFET technology. The simulations include dc gain, phase margin, common mode rejection ratio (CMRR), input common mode range (ICMR), slew rate and noise analysis. Simulations have been performed with a 0.8 V supply voltage, 80nA bias current and 0.2 pF load capacitance.

The sizing of the transistors was obtained using inverse coefficient (IC) methodology. There are three inversion levels of transistor strong, moderate and sub-threshold inversions. These levels are related to gate to source voltage (VGS), transistor size (W/L), and drain current (ID). The IC is given by

$IC=I_D/(I_O (W/L))$ ----------(23)

Where I_O is the function of process and is equal to

$I_O=2n\mu Cox\ U_T^2$

Where U_T is the thermal voltage of the semiconductor, Cox is the gate oxide capacitance per unit area, μ is the carrier mobility, and n is a substrate factor. Table 1 gives relationship between inverse coefficient and inversion levels.

Table 1: Inversion Level vs inverse coefficient

Region	IC
Strong Inversion	>10
Medium Inversion	0.1-10
Sub-threshold	<0.1

For proper operation, the (W/L) of upper transistor is higher than the smaller than the lower transistor. To achieve the sub-threshold operation of device (IC < 0.1) the number of fins of upper transistor is higher than the lower transistor with same length (L=30 nm), operating at low bias current (100 nA) and the threshold voltage (VTH) is greater than gate to source voltage (VGS)

Table 2 demonstrates the process parameters of the FinFET. Table 3 demonstrates the dimensions of transistors. For all FinFETs length is chosen 30 nm and width is formulated by

$W = n (T_{fin} + 2 * H_{fin})$ ---------(24)

Where n = number of fins
T_{fin} = Fin Thickness
H_{fin} = Fin Height

Table 2: Process parameters of the FinFET 18 nm Technology

Parameter	N-FinFET	P-FinFET
Length(nm)	18	18
Fin Height (nm)	35	35
Fin Thickness (nm)	12	12
Threshold Voltage(V_{TH})	0.28	-0.261
Supply voltage(V)	0.8	0.8

Table 3: Dimensions of the transistor

Transistor	Type of FinFET	Length (L) in nm	Number of fins
M1x-M2x	N	30	10
M1y-M2y	N	30	1
M3x-M4x	P	30	20
M3y-M4y	P	30	2
M5x	N	30	10
M5y	N	30	1
M6x	P	30	20
M6y	P	30	4
M7x	N	30	10
M7y	N	30	2
M8x	N	30	10
M8y	N	30	1

The proposed and conventional OTA frequency showing gain and phase response is plotted in Fig.7 and Fig.8.

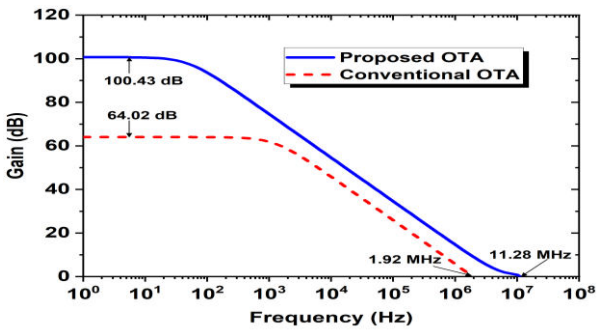


Fig. 7. Simulated Two OTA's open loop frequency response

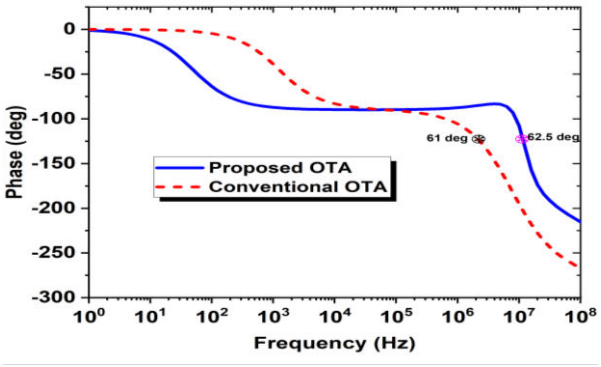


Fig. 8. Simulated phase response of Two OTA's

The dc gain of proposed OTA circuit was 100.43 dB which was 36.41 dB higher than that of conventional OTA. With indirect frequency compensation technique the compensation capacitor (CM) is less that of conventional OTA and also left half plane (LHP) adds the phase response to improve the stability.

The common mode rejection ratio (CMRR) is given as

$$CMRR = 20\log_{10}\frac{A_{DM}}{A_{CM}}$$

Higher the CMRR is better to suppress the common mode input signals. Simulated two OTAs CMRR is shown in Fig.9. The proposed OTA has CMRR of 30 dB higher than the conventional OTA at lower frequencies.

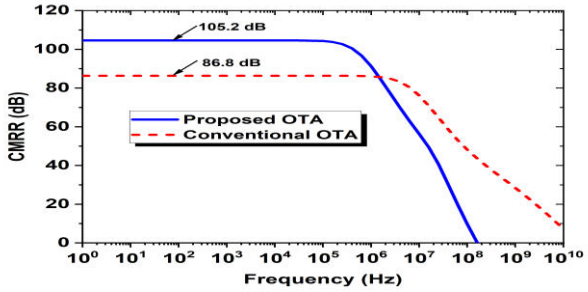


Fig. 9. Simulated CMRR of Two OTA's

Fig.10 shows the simulate DC transfer characteristics of two OTAs in unity gain configuration. The applied voltage (V_{IN}) at non-inverting input was varied from 0 V to 0.8 V. The output voltage of the proposed OTA ranged from 131.04 mV to 788mV.33 mV difference in minimum allowable input voltage was observed due to V_{DSat} of tail current source composite cascode structure M5x-M5y.

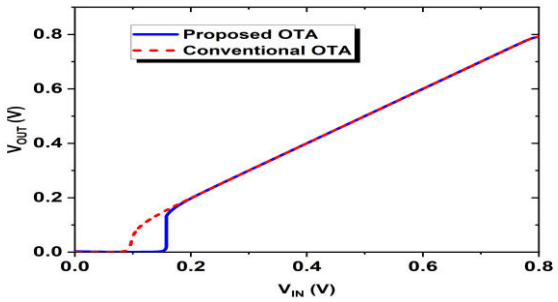


Fig. 10 Simulated ICMR of Two OTA's

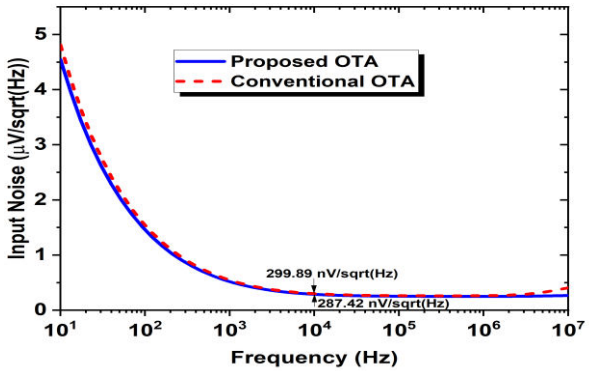


Fig. 11. Input referred noise simulation of two OTAs.

Noise simulations of two OTAs are shown in Fig.11. The noise is mainly in the low frequency band, decreases with increasing frequency and eventually stabilizes. The noise of a two stage OTA is dominated by the input impedance of first stage. The input referred noise voltage of the proposed OTA measured at 10 KHz is 287.42nV/√Hz.

Slew rate indicates the OTA speed. It mirrors the output voltage of proposed OTA circuit to follow the changes in the input voltage. This is obtained from the capacitor C_M current. The time varying input and output voltages for simulating proposed OTA is shown in Fig.12. The simulated value of slew rate of proposed OTA is 2.7V/(μsec) and that of conventional OTA is 1.1V/(μ sec).The improvement of slew rate in proposed OTA due lower value of compensation capacitor (C_M).

The comparative performance of proposed OTA and Conventional OTA with recent works is shown in table.4. The FinFET based two stage OTA with composite cascode technique achieved high dc gain than the reported data. Based on power dissipation, speed and gain, the figure of merit (FOM) is given for OTAs as

$$FOM=\frac{DC\ GAIN.UGB}{Power\ dissipation}\text{--------}\ (25)$$

The proposed circuit has highest FOM among the reported data due lower compensation capacitor with indirect frequency compensation technique.

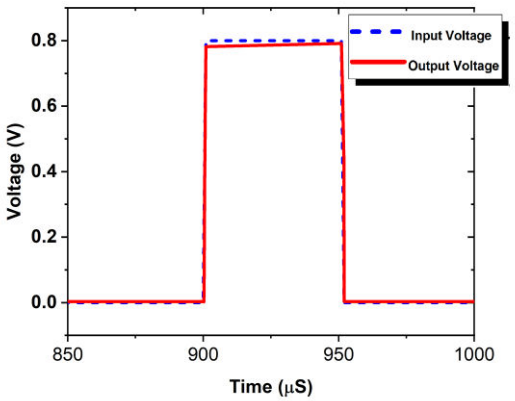


Fig. 12. Slew rate of proposed OTA circuit.

Table 4: Comparative performance of proposed work with reported data

Parameter	Ref[22]	Ref[23]	Ref[21]	Ref[18]	Conventional OTA	Proposed OTA
Technology	CMOS 130 nm	IGFinFET 55 nm	FinFET 16 nm	FinFET 30 nm	FinFET 18 nm	FinFET 18 nm
Supply voltage(V)	0.8	1	1.8	1.0	0.8	0.8
Bias current (nA)	-	-	-	20	80	80
DC Gain (dB)	74.1	45.51	23.7	57.8	64.02	100.43
Phase margin (deg)	61	60.1	--	69.81	61	62.5
Unity Gain Bandwidth (MHz)	4.75	63	5200	13.17	1.9	11.28
CMRR (dB)	109	59.65	76.67	61.55	86.8	105.2
Input referred noise ($\frac{nV}{\sqrt{Hz}}$)	115	300	-----	153.27	299.99	287.42
Slewrate ($\frac{V}{\mu sec}$)	1.27	41.34	17,500	0.42	1.1	2.7
Power dissipation (nW)	11200	6480	537100	108	192	128
FOM ($\frac{dB.MHz}{\mu W}$)	0.031	0.442	0.22	7.04	0.63	8.85

5. Conclusion

In this paper, a composite cascode based two stage OTA is designed using FinFET devices in sub-threshold region of operation for high gain and low power. The inversion coefficient design methodology provides gain optimization and low power consumption. The proposed OTA achieves 100.43 dB, and a phase margin of 62.50 with supply voltage of 0.8 V and 80 nA bias current. It OTA realizes UGB of 11.28 MHz, CMRR of 105.2db,

input referred noise of 287.42nV/√Hz, slew rate of 2.7 V/(μsec) and power dissipation of 160 nW. The proposed circuit has best FOM of 8.85 (dB MHz)/μW among the reported data suitable for biomedical applications.

REFERENCES

1. E. Lopez-Morillo et al., "A 1.2-V 140-nW 10-bit Sigma–Delta Modulator for Electroencephalogram Applications," *IEEE Trans. on Biomedical Circuits and Systems,* vol. 2, no. 3, pp. 223-230, Sept. 2008,
2. J. Comer, D. T. Comer and R. P. Singh, "A high-gain, low-power CMOS op amp using composite cascode stages," *2010 53rd IEEE International Midwest Symposium on Circuits and Systems, 2010,* pp. 600-603
3. J. Nowak et al., "Turning silicon on its edge double gate CMOS/FinFET technology]," *IEEE Circuits and Devices Magazine*, vol. 20, no. 1, pp. 20-31, Jan.-Feb. 2004,.
4. G. Raikos, S. Vlassis, C. Psychalinos, "0.5V bulk-driven analog building blocks, "*AEU - International Journal of Electronics and Communications*, Volume 66, Issue 11,2012,Pages 920-927,ISSN 1434-8411,
5. Khateb, Fabian. "Bulk-driven floating-gate and bulk-driven quasi-floating-gate techniques for low-voltage low-power analog circuits design." *AeU-international Journal of Electronics and Communications* 68 (2014): 64-72.
6. S. S. Rajput and S. S. Jamuar, "Low voltage analog circuit design techniques," *IEEE Circuits and Systems Magazine*, vol. 2, no. 1, pp. 24-42, 2002.
7. YAN, S., SANCHEZ-SINENCIO, E. Low voltage analog circuit design techniques: A tutorial. *IEICE Trans. Analog Integrated Circuits and Systems*, vol. E00–A, no. 2, 2000.
8. Zabihian, Saeid & Lotfi, Reza, "A sub-1-V high-gain single- stage operational amplifier," *IEICE Electronic Express*. 5, 211-216. 10.1587/elex.5.211, 2008.
9. Rishi Pratap Singh, David J. Comer, Taylor Waddel, Donald T. Comer & Kent Layton, "High-gain microwatt composite cascode op amps," *International Journal of Electronics*, 99:9, 1179-1190,
10. Comer, David & Comer, Donald & Petrie, Craig., "The utility of the composite cascode in analog CMOS design," *International Journal of Electronics*, 91, 491-502, 2004.
11. Gray, Paul R. and Robert G. Meyer. "MOS operational amplifier design-a tutorial overview." *IEEE Journal of Solid-State Circuits* 17, pp. 969-982, 1982.
12. Hurst, Paul & Lewis, Stephen & Keane, John & Aram, Farbod & Dyer, Kenneth, "Miller Compensation Using Current Buffers in Fully Differential CMOS Two-Stage Operational Amplifiers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 51, pp. 275 – 285, 2004..
13. V. Saxena and R. J. Baker, "Indirect feedback compensation of CMOS op-amps," *2006 IEEE Workshop on Microelectronics and Electron Devices,* 2006. WMED '06., 2006, pp. 2 pp.-4.
14. M. Tan and W. -H. Ki, "Current-mirror miller compensation: An improved frequency compensation technique for two-stage amplifiers," *2013 International Symposium on VLSI Design, Automation, and Test (VLSI-DAT),* pp. 1-4, 2013.
15. B. Nauta and AJ. Annema, "Analog/RF circuit design techniques for nanometerscale IC technologies," *Proceedings of the 31st European Solid-State Circuits Conference, 2005 (ESSCIRC 2005).*pp. 45-53,

C. Hisamoto et al., "FinFET-a self-aligned double-gate MOSFET scalable to 20 nm," *IEEE Transactions on Electron Devices*, vol. 47, no. 12, pp. 2320-2325, Dec. 2000,.

16. Q. Xie, CJ. Lee, J. Xu, C. Wann, J. YC. Sun and Y. Taur, "Comprehensive Analysis of Short-Channel Effects in Ultrathin SOI MOSFETs," *IEEE Transactions on Electron Devices*, vol. 60, no. 6, pp. 1814-1819, June 2013,
17. Sonkusare, Reena & Pilankar, Prathamesh, Rathod SS, "Analysis of sub-threshold SOI FinFET-based two-stage OTA for low power," *Analog Integrated Circuits and Signal Processing*, vol. 98, 2019
18. Thakker, Rajesh & Srivastava, Mayank, Tailor, Ketankumar & Shojaei Baghini, Maryam, Sharma, Dinesh, Rao, Vinjamuri , B., Mahesh, "A novel architecture for improving slew rate in FinFET-based op-amps and OTAs," *Microelectronics Journal,* vol. 42: 758-765, 2011
19. Kori PK, Dixit A, Rajan C, et al., "22 nm LDD FinFET Based Novel Mixed Signal Application: Design and Investigation," *Silicon*, 2022.

20. J.K. Kasthuri Bha, P. Aruna Priya, "Low power & high gain differential amplifier using 16 nm FinFET, " *Microprocessors and Microsystems*, vol. 71, 2019, 102873. ISSN 0141-9331,
21. Hassanzadeh, A., Hadidi, S., "Systematic approach for IG-FinFET amplifier design using gm/Id method," *Analog Integr Circ Sig Process vol.* 109, pp. 379–385, 2021.
22. Bai, Na, Xiaolong Li, and Yaohua Xu, "A Low-Voltage, Ultra-Low-Power, High-Gain Operational Amplifier Design for Portable Wearable Devices," Electronics, vol. 11, no. 1, pp. 74, 2022