A Novel Coupled Pyramid Inductor for High Figure of Merit VCO Design for Telemetry Transponder Applications

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Abstract:

Problem: The improvement in the performance of VCO can be achieved by increasing the quality factor of the resonant tank circuit. Especially, the inductor quality factor affects the quality factor of the circuit and phase noise of the VCO. **Approach:** This paper presents a compact coupled pyramid inductor for the design of VCO, amplifier, and filter applications. The inductor is designed using Sonnet software in a pyramid and coupled pyramid structure to reduce the capacitive parasitics and losses. Furthermore, the inductance and quality factor of the coupled inductor is enhanced by tapering the width of the conductor and stacking the metal layers to reduce substrate losses and eddy current losses. **Findings:**The effect of quality factor and inductance are validated by designing a VCO at 3.15 GHz. The simulated best phase noise for the VCO is -125 dBc/Hz @ 1MHz, and the figure of merit is -216 dBc/Hz at 1 MHz offset. **Conclusion:** The proposed coupled pyramid inductor achieves better output power, tuning range, and figure of merit, which makes it a good candidate for applications in the design of filters, amplifiers, oscillators, and receiver circuits for various wireless communication systems and telemetry transponders.

Key words: Figure of merit, multi-path techniques, phase noise, Q-factor, voltage controlled oscillator.

1. Introduction

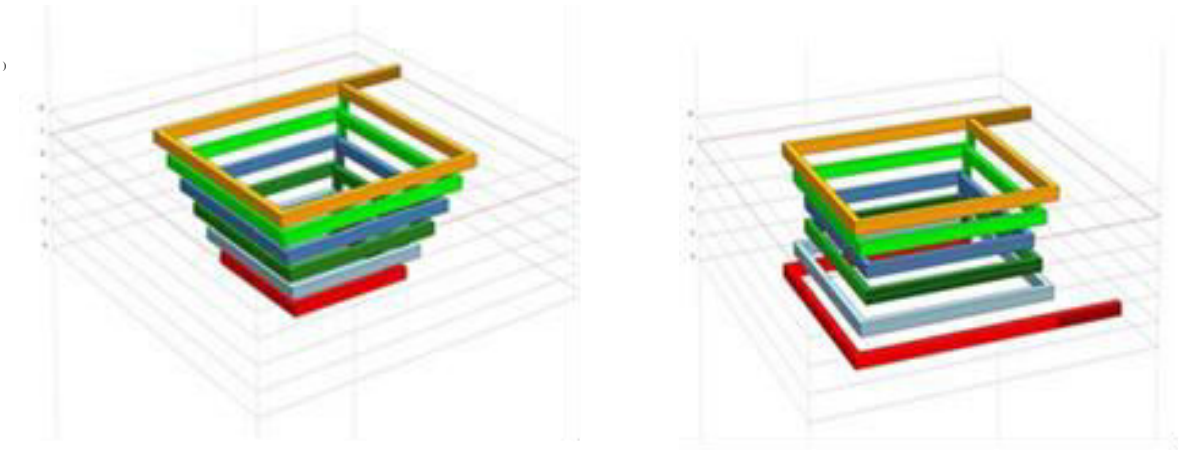
On-chip inductors are used in many applications like filters, matching networks, Phase Locked Loop (PLL) and tuning circuits, etc., which require high-quality factors at high frequencies. Integrating the inductor on-chip with high inductance is still a highly challenging task. The quality factor of the on-chip inductor will be limited mainly due to substrate loss, resistive loss, and eddy current loss [1, 2]. The quality factor and inductance of on-chip inductors are affected by the variation in conductor width, spacing between conductors, and the number of turns [3].Several techniques have been employed to improve the performance of the inductors such as using different geometries, shielding, stacking layout techniques, loss reduction techniques, etc. [4]. The inductor's size and shape impact the quality factor, and circular inductor and octagonal inductors provide the best quality factor due to their small footprint and lower substrate losses. Coupling among the metallic strips of the inductor reduces the quality factor and the self-resonant frequency. To overcome this,a patterned ground structure is used, which provides a shielding effect reducing the capacitance to ground, conductive loss of the metal track, and the dielectric loss of the substrate [5]. It also reduces the turn number for the inductor due to the shielding effect. Parasitic capacitance in inductors reduces the self-resonant frequency and degrades the performance of the inductors when used in VCO applications. A high inductance inductor can be achieved in stack inductor design due to the self-inductance and mutual inductance of the structure [6]. To enhance the quality factor in stacked inductors taper structure is employed [7]. The taper structure reduces the eddy current, and the varying line width and spacing dimensions increase the stored energy and hence the quality factor. Another parameter that reduces the quality factor is the current crowding effect, and this can be reduced by designing the inductors to carry current in multi-paths [8]. The current flowing in opposite paths produces

opposing magnetic fields, reducing current crowding and enhancing the quality factor. However, the multi-path method may not always be useful as the inner paths are shorter and the outer paths are large [9]. Metal stacking can be utilized to improve the quality factor. The two twisted loops produce magnetic fields of equal magnitude and opposite polarities, reducingthe current crowding effect and enhancing the quality factor.

The signal generation in a communication system is achieved using phase-locked loops (PLL) or synthesizers. In PLLs, VCO is a vital component that is the source of RF power. The specifications of VCO are becoming critical with the development of technology. The required characteristics are compact size, low phase noise, low DC power requirement, wider tuning frequency, etc. The figure of merit (FoM) encompasses the above parameters to compare the performances of VCOs. A CMOS LC oscillator using tail current shaping is designed to improve the phase noise [10]. The oscillator exhibits a 7.7 dBc/Hz improvement in phase noise over the classic oscillator. The FoM achieved for the oscillator at an offset of 1MHz is -193 dBc/Hz. A low-cost VCO with a FoM (-188.9 dBc/Hz) at 1MHz offset is designed with a dc power requirement of 2.5mW [11]. A quadrature VCO for high performance using a symmetric differential inductor is designed in [12]. The VCO exhibits an FoM of -184.6 dBc/Hz. A VCO with a tunable active inductor is designed in [13]. The VCO is implemented in the differential form to provide compact, low-power consumption performance; however, the FoM is -143 dBc/Hz. An ultra-low phase noise VCO is designed in class B topology [14]. The VCO with a FoM of -139.44 dBc/Hz is designed for 1.6 GHz.
This paper proposes a novel pyramid and coupled pyramid inductor in multilayer configuration. The coupled pyramid inductor reduces the capacitive parasitic and eddy current, improving the inductance and quality factor. This is achieved by designing the inductor in multilayers, and the width of the strip is reduced with the progression of the layers. The organization of the proposed paper is as follows: Section 2 describes the pyramid and coupled pyramid inductor structures. Sonnet simulations are presented in section 3. Section 4 proposes the coupled pyramid inductor for the design of a resonant circuit in VCO. Section 5 presents the conclusion and applications.

2. Proposed pyramid and coupled pyramid inductor structure

The proposed inductor is designed to enhance the inductance and quality factor. Calculation of inductance is critical in the design of on-chip inductor. The total inductance can be calculated as the series inductance of individual conductors and mutual inductance. When the current is carrying in the same direction, the positive coupling and inductance increase; when in two metal tracks, currents are flowing in opposite direction and placed close to each other, the overall inductance decreases. The effect of self and mutual inductance on the overall dcinductance of the inductor is discussed in [2]. The pyramid inductor is designed such that the inner diameter is varied from top to bottom layer. As the layer increases the inner diameter decreases by 2um. To improve the inductance, two turns are taken at each layer and in every layer variable width and dimension are taken to increase the quality factor of the proposed inductor as shown in Fig. 1(a).The pyramid inductor is designed with a conductor width of 2 um, the spacing between the conductor is 0.5um and the thickness of the conductor is 2um. The outer diameter of the inductor is reduced as the inductor is designed in the lower metal layers. This reduces the field coupling between the adjacent layers and improves the substrate losses due to field coupling and displacement current.
The coupled pyramidal inductor is designed similarly to the pyramid inductor as shown in Fig. 1(b); however, in this case the outer diameter is reduced till three bottom layers and then increased symmetrically for the next three layers. The stacked structure further reduces the substrate loss and field coupling, increasing the inductance and quality factor. The width of the conductor is 2um, the gap between the conductors is 0.5um, and the thickness of the conductor is 2um. The stacking of the metal strips symmetrically reduces the eddy current loss and crowding effect by reducing the magnetic fields entering the substrate.



(a) (b)

Figure1.(a)Pyramidinductor(b)Coupledpyramidinductor

3. Simulated results of the pyramid and coupled pyramid inductor

The proposed inductor is EM simulated using SONNET simulation tool to confirm the increase in inductance and quality factor. The pyramid and coupled pyramid inductor is designed on Silicon substrate with 100um thickness. The inductance, quality factor, and resistance are calculated using eq. (1-3) from the Y parameters. These Y- parameters are converted from S-parameters.

$$L = \frac{1}{2\pi f}\,\mathrm{Im}\left[\frac{1}{Y_{11}}\right] \qquad (1)$$

$$Q = -\frac{\mathrm{Im}\left[\frac{1}{Y_{11}}\right]}{\mathrm{Re}\left[Y_{11}\right]} \qquad (2)$$

$$R_s = \frac{1}{\mathrm{Re}\left[Y_{12}\right]} \qquad (3)$$

The above parameters are shown in Fig. 2 and Fig. 3. The simulation results exhibit a marked improvement in the inductance value of the coupled pyramid inductor over the pyramid inductor. The quality factor improvement is marginal. However, the higher inductance value is used to design inductors at lower frequencies. A compact inductorcan be used for obtaining the higher value of inductance using coupled pyramid inductor. The simulation values achieved for the pyramid and coupled pyramid inductor are shown in Table 1.

Table 1.Comparison of the Pyramid and Coupled pyramid inductor

Parameter	Pyramid	Coupledpyramid
Inductance(nH)	1.92	4.85
Peak qualityfactor	16.8	17.15

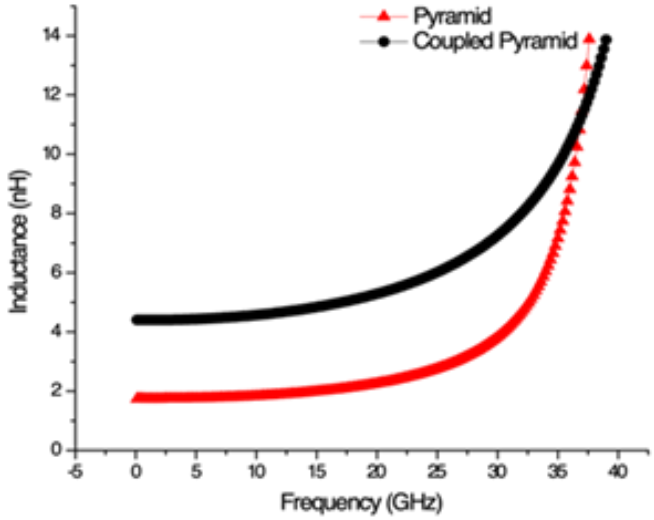


Figure 2. Pyramid and coupled pyramid inductance comparison

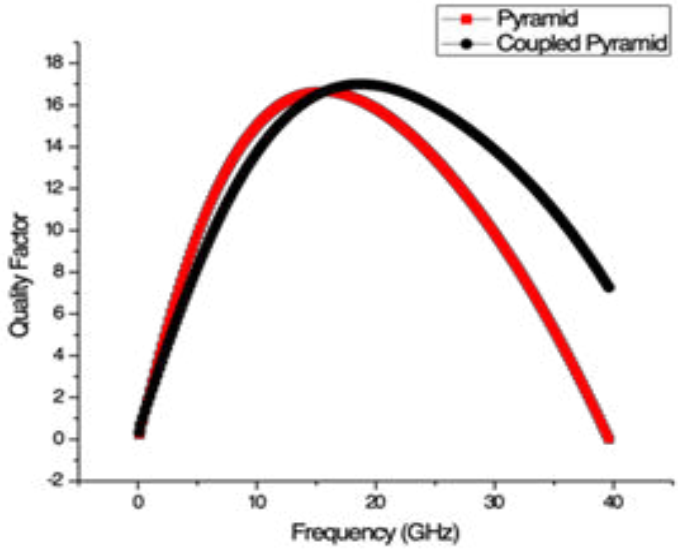


Figure 3. Pyramid and coupled pyramid Q-factor comparison

4. VCO Design with Coupled Pyramid Inductor Structure

The designed inductor finds applications in amplifiers, VCOs, and filters. In this paper, the performance of the coupled inductor is assessed by using it in the resonant tank circuit of a VCO. The Clapp configuration is used to design the basic oscillator, as it performs better at higher frequencies. The oscillator is then tuned

using a varactor diode to vary the output frequency. The Clapp oscillator consists of an amplifier in a common emitter configuration, providing the requisite gain and 180^0 phase shift. The resonant circuit providesan additional 180^0 phase shift to satisfy Bark Hausen criteria as shown in Fig. 4. The coupling capacitors at the input and output of the amplifier are used to block DC bias from disturbing the source and load. The design steps for the Clapp oscillator are given in Ref [16]. The design is based on the above reference. The frequency of oscillation for the circuit is dependent on the inductor and the varactor capacitance and is given as

$$\omega_0 = \frac{1}{\sqrt{L_{cpi} C_{\text{var}}}}$$

Lcpi is the inductance of the coupled inductor and Cvar is the tunable varactor diode capacitance.

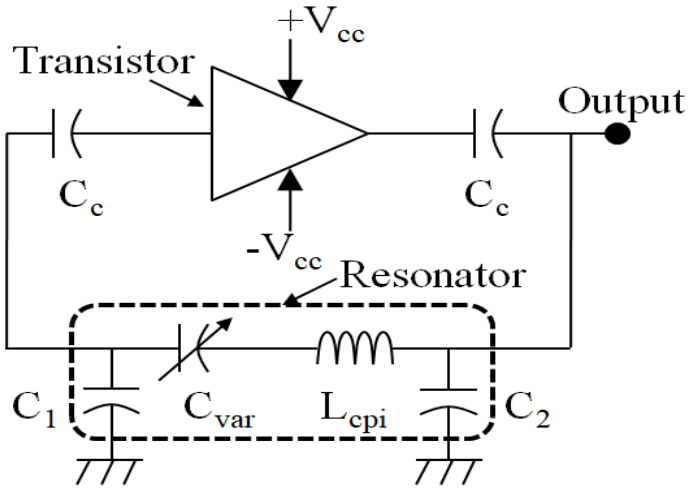


Figure 4. Block diagram of VCO in Clapp oscillator

The varactor diode capacitance is varied by applying a reverse bias across the diode, and as the voltage is increased, the capacitance of the varactor diode decreases. SMV2019-040LF varactor diode is used whose capacitance varies from 0.4 pF to 1.8 pF for change in bias voltage from 0 V to 15 V. The figure of merit for the oscillator is defined as shown in eq. (5) [16].

$$FoM = L\{\Delta f\} - 20\log_{10}\left(\frac{f_0}{\Delta f}\right) + 10\log_{10}\left(\frac{P_{dc}}{1mW}\right) \quad (5)$$

Where f_0 is the centre frequency, L $\{\Delta f\}$ is the phase noise, Δf is the tuning bandwidth, and P_{dc} is the DC power dissipation.

The biasing circuit consists of a lowpass filter and a resistor to control the current. The lowpass filter blocks the RF signal from entering the DC supply. The transistor source is grounded using multiple vias as shown in Fig. 5. Theinput and output capacitors block the DC from leaking through resonator and load

resistance.The S-parameters of the coupled inductor are imported from SONNET software and used in the schematic for the resonator circuit and the varactor spice modelis used. This circuit selects the output frequency of the oscillator. The tuning capacitance determines thetuning ranging for the VCO.

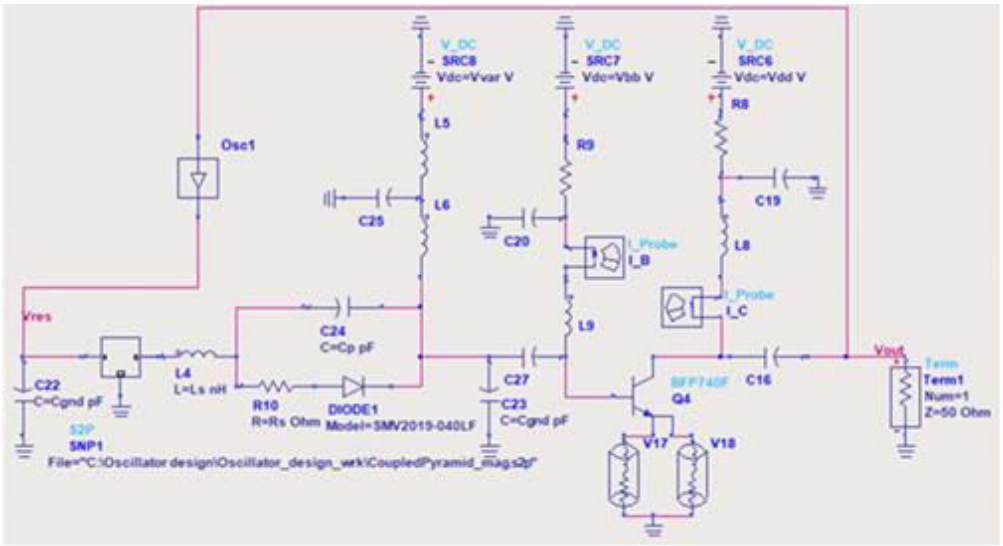


Figure 5. Circuit diagram of the VCO in Clapp oscillator configuration

The simulated output spectrum of the VCO is shown in Fig. 6. The output power of the VCO is 7.56 dBm. The tuning range of the VCO is shown in Fig. 7. It is observed that the capacitance variation in the varactor results in a frequency change from 2.75 GHz to 3.59 GHz. The frequency tuning range is 0.84 GHz which is 26.4% of the centre frequency. The output power variation is shown with frequency in Fig. 8. It is observed that the power is constant till 3.3GHz, and the power falls off to 4.5 dBm at 3.59 GHz.

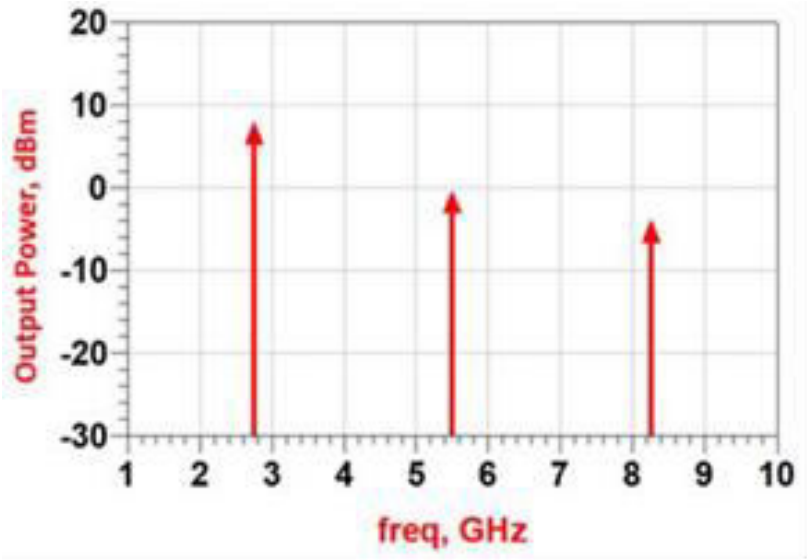


Figure 6. Output VCO Spectrum

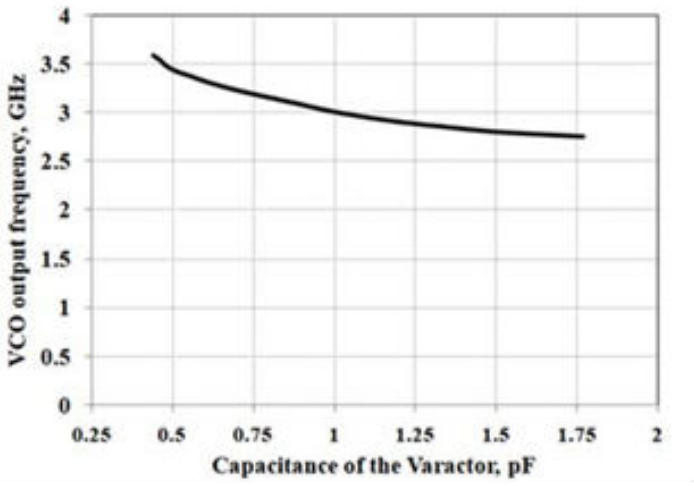


Figure 7. VCO output frequency variation over Varactor capacitance

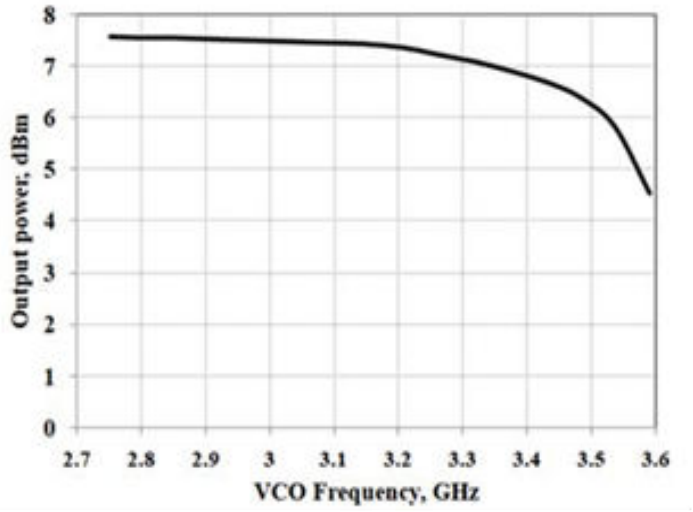


Figure 8. Output power over the frequency band of VCO

The VCO phase noise and FoM results are shown in Fig. 9 at 2.75 GHz. It is observed that the VCO exhibits a phase noise of -65.55 dBc/Hz at 1 KHz offset, -125.55 dBc/Hz at 1 MHz offset, and FoM of -215.47 dBc/Hz at 1MHz offset. The phase noise and FoM values exhibited by the VCO are due to improved quality factors and higher inductance values in compact size. This shows that the coupling effects and the losses have been suppressed with the coupled pyramid inductor. The variation of phase noise at 1 KHz offset is shown in Fig. 10; it is observed that the phase noise increases as the output frequency increases due to changes in the resonator's quality factor. Finally, the Phase noise and FoM at 1MHz are plotted for output frequency in Figure 11. The variation is as predicted due to changes in the Q-factor of the resonant circuit.

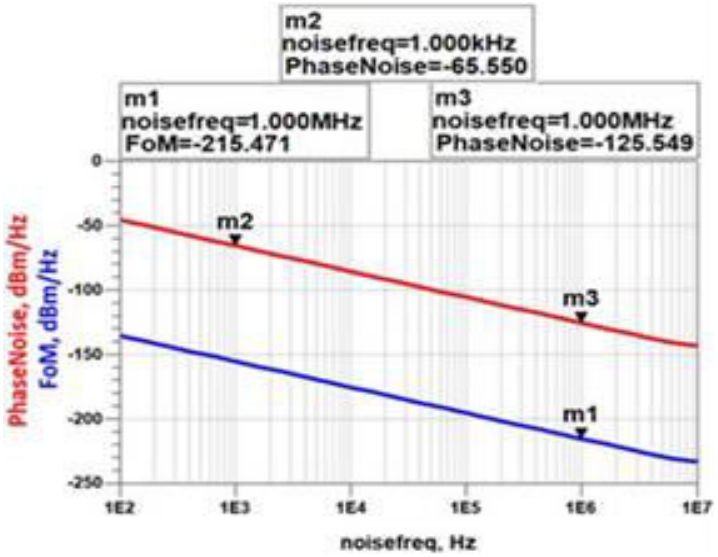


Figure 9. VCO phase noise and Figure of merit (FoM) at 2.75 GHz

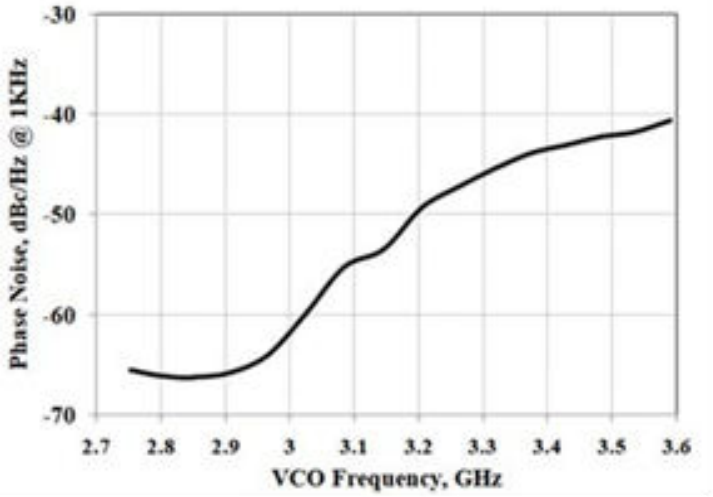


Figure 10. Phase noise at 1 KHz offset over the frequency band of VCO

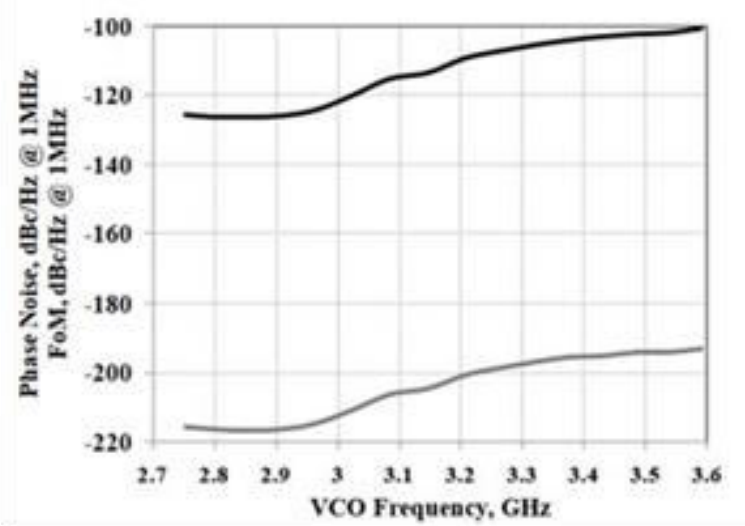


Figure 11. Phase noise and FoM over the frequency band of VCO

The comparison of the performance parameters of the proposed VCO with other reported structure is shown in Table 2. The output power of the 7.43 dB at centre frequency is higher than other designs,

however, the power dissipation is slightly higher than other designs. This is compensated with the output power. The tuning range for the reported VCO is 26.4% whereas for ref [13] it is 20%. The phase noise of the proposed VCO at 1 KHz offset is better than ref [10] at - 53.5dBc/Hz. The FoM considers all the important parameters of the VCO such as phase noise, tuning range, centre frequency and power dissipation, hence, gives the overall performance parameter of the VCO and is an important factor in comparison of the VCOs. The FoM of the proposed VCO is -204.5 dBc/Hz @ 1 MHz offset, which is the best among the reported VCOs.

Table 2. Comparison of reported VCOs with this work

Parameter	[11]	[12]	[13]	[15]`	This Work*
Supply Voltage (V)	-	1.8	1.2	3.3	1.2
Power Consumption (mW)	1.5	7.3	5.4	-	7.68
Tuning Range (GHz)	3.6	2.506	4.5-5.5	1.6	2.752-3.59
Output power (dBm)	-	-9.8	-	-	7.43
PN dBc/Hz @ 1 KHz	-45	-	-	-	-53.5
PN dBc/Hz @ 1 MHz	-118.2	-123.7	-119.7	-139.4	-113.5
FoM dBc/Hz @ 1 MHz	-189.9	-188.9	-184.6	-184	-204.5

5. Conclusion

In this paper, a pyramidal inductor is designed and subsequently modified to a coupled pyramid inductor in multilayer technology. The width of the coupled pyramid inductor is modified to decrease the eddy currents and the substrate losses. The inductance and quality factor enhancementare observed in the coupled pyramid inductor. The inductor's performance is validated by designing the resonant circuit in VCO design. The VCO exhibits the best FoM of -218 dBc/Hz at 1 MHz offset at lower frequencies and -204.5 dBc/Hz at 1 MHz offset at the centre frequency. The VCO output power is also higher at 7.5 dBm. The inductor finds applications in the design of filters, amplifiers, oscillators, and receiver circuits for various wireless communication systems.

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